BỘ GIÁO DỤC VÀ ĐÀO TẠO
TRƯỜNG ĐẠI HỌC SƯ PHẠM KỸ THUẬT
THÀNH PHỐ HỒ CHÍ MINH

TRẦN VĨNH THANH

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DANH MỤC CÁC BÀI BÁO ĐÃ CÔNG BỐ

Tp. Hồ Chí Minh, tháng năm 2023

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Phản biện 2:

Phản biện 3:

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CÁC CÔNG TRÌNH ĐÃ CÔNG BỐ

[1] D. -T. Do, V. -T. Tran, M. -K. Nguyen and S. Naik, "Fault Tolerant Control Methods for Three-Level Boost T-Type Inverter," *IEEE Transactions on Industrial Electronics*, 2022.

[2] Duc-Tri Do, Vinh-Thanh Tran, Minh-Khai Nguyen. An DPWM for Active DC-Link Type Quasi-Z-Source Inverter to Reduce Component Voltage Rating. *Energies*, vol. 15, no. 13, pp. 4889, July 2022.

[3] V. -T. Tran, M. -K. Nguyen, D. -T. Do and Y. -O. Choi, "Space Vector Modulation Method-Based Common Mode Voltage Reduction for Active Impedance-Source T-Type Inverter," *IEEE Access*, vol. 10, pp. 10149-10159, 2022.

[4] Duc-Tri Do, Vinh-Thanh Tran, Minh-Khai Nguyen. Enhanced Boost Factor for Three-Level Quasi-Switched Boost T-Type Inverter. *Energies*, vol. 14, no. 13, pp. 3920, May 2021.

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Fault Tolerant Control Methods for Three-Level Boost T-Type Inverter

Duc-Tri Do, Vinh-Thanh Tran, Minh-Khai Nguyen, *Senior Member, IEEE*, and Sanjeev M. Naik, *Senior Member, IEEE*

***Abstract*—This article presents control techniques for three-level boost T-type inverter (TLB-T^{2}I) to address open-circuit faults (OCFs) and short-circuit faults (SCFs) of semiconductor devices. Three main groups of semiconductor failures of TLB-T^{2}I are OCFs of boost switches (*F*1), OCFs of inverter half bridge switches (*F*2), and OCFs of bidirectional switches (*F*3). Under the proposed approaches, the inverter generates a two-level output voltage with the *F*1 and *F*2 faults, while it still generates a three-level output voltage with the *F*3 fault. These control techniques are extended to solve OCF and SCF of diodes, SCF of boost switches, and OCF of capacitors. Operating modes of the inverter in both normal and fault conditions are presented. Design guidelines, power loss contribution, and comparison study are included. The experimental results based on a 1-kVA prototype are carried out to verify the accuracy of the proposed methods. The result shows that the proposed methods can reduce component voltage ratings when compared to the conventional methods. In particular, the voltage rating of the inverter half-bridge switch in the *F*2 fault-tolerant method is reduced by at least 50% compared to the traditional techniques.**

***Index Terms*—Fault-tolerant (FT), open-circuit fault (OCF), space-vector modulation, three-level boost (TLB) inverter, t-type inverter.**

I. Introduction

In RECENT years, inverters based on fast semiconductor devices have provided good performance because of their advantages, such as high-power density, high efficiency, and good output power quality [1]. However, these power switching devices have a high failure rate. Solving semiconductor failure can improve the system reliability, especially in some applications as an uninterruptable power supply. Semiconductor failures can be classified into two main groups: open-circuit fault (OCF) and short-circuit fault (SCF). The reasons for these failures are discussed in [2]–[4]. In general, the SCF is more serious than the OCF and usually leads to destroy the system due to the high short-circuit current. Then, the system is usually forced to stop for safety whenever SCF is detected. An impedance-source network can be installed before a conventional voltage source inverter to limit the amplitude of SC current [5]–[7]. It gives the system more time to handle the SCF. In contrast to the SCF, the inverter can keep operating by using appropriate modulation techniques when the OCF occurs. Thus, the solving OCF problem has attracted many researchers. Many studies about OCF diagnosis [8]–[11] and fault-tolerant (FT) methods [12]–[31] have been proposed. These methods provide many fast and exact detection methods for the OCF. Especially, the work in [8] can detect the OCF within 10 μs.

The FT methods for OCF are usually applied to multilevel inverters [12]–[34]. A seven-level cascaded H-bridge inverter with fault tolerant capability is introduced in [12]. In this article, the faulty H-bridge is bypassed to isolate failed semiconductor devices. Active switches are installed at the output terminals of the H-bridge circuit to make short circuit the output voltage of faulty submodule. As a result, the amplitude of output voltage is decreased in post-fault operation. Besides the cascaded topology, T-type inverter topology is an attractive structure for implementing FT methods [13], [14]. However, the magnitude of the output voltage is also reduced when the FT scheme is activated [13], [14].

The conventional three-level T-type inverter with FT capability has received a lot of attention from researchers. In this topology, a single OCF can occur at either upper, lower, or bidirectional switches. The OCF of the bidirectional switch produces not only a small degradation of the output current quality but also unbalanced capacitor voltages. This OCF can be easily addressed by modifying the modulation schemes [15]–[17]. In these studies, the faulty phase operates as a two-level inverter with the help of upper and lower switches, while the other healthy phases operate as in normal condition. In particular, the methods in [15] and [16] provided capacitor voltage balancing under fault condition. When the OCF occurs at the upper or lower switch of the T-type inverter, the positive or negative half cycle of output current is not achieved. It generates a serious distortion at the output current. The system must be stopped if the FT solution is not applied. Two main solutions for the case of OCF include using additional hardware circuits [18]–[27] and appropriate pulsewidth modulation (PWM) techniques [26]–[31]. The simplest way to recover inverter operation in single

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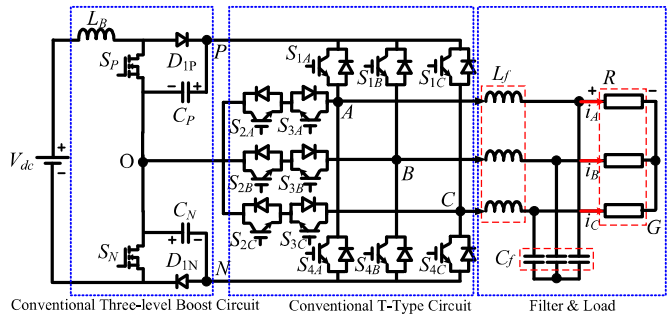

Fig. 1. Topology of conventional TLB-T^{2}I [32].

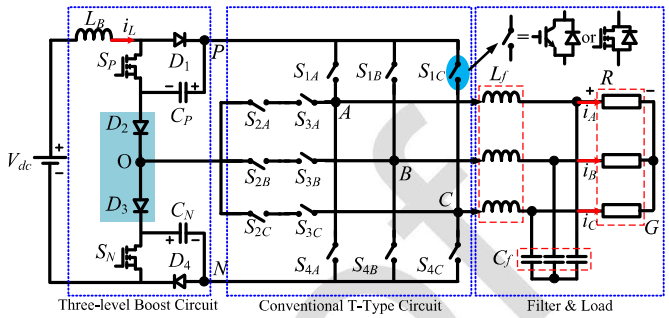

Fig. 2. Topology of TLB-T^{2}I.

or multiple semiconductor OCFs is to use two parallel inverters [18]–[21]. However, this solution requires a large number of switching devices. Another solution is to use an additional inverter redundant leg as presented in [22]–[25]. In [22] and [23], one extra T-type branch was installed before the main T-type inverter. The bidirectional switch of redundant leg was always turned ON to connect the dc-link mid-point to the main inverter in normal condition. In post-fault operation, this bidirectional switch is turned OFF to isolate the main circuit from the neutral point. Then, the inverter operates as a two-level inverter. The bidirectional switches of the main T-type circuit and upper or lower switches of the redundant leg help to continuously provide energy to the load. The works in [24] and [25] introduced a novel redundant leg consisting of two active switches and six diodes. The main T-type circuit of this solution was also modified, which used six extra diodes for inner switches. In post-fault operation, this inverter also produces a two-level voltage at output terminals. In general, the hardware-based solution brings many benefits such as ensuring full output power rating and solving multiple OCFs. However, it requires many additional semiconductor devices as well as the inverter only operates in buck mode.

The other solutions in [26]–[29] are based on PWM control techniques. In the reports in [26] and [27], bidirectional switches of faulty phase are turned ON to clamp the output terminal to the mid-point of input voltage. The other healthy phases with modified modulation signals help to recover output voltages. The study in [28] used inner and lower switches to solve the OCF of upper switches. In [28], the inverter operation degrades from three levels down to two levels. These methods do not require any extra semiconductor devices. However, in [26]–[28], the amplitude of the output voltage is reduced by half compared to the normal condition. To ensure desired output voltage, a dc–dc boost converter should be installed before the inverter to boost the dc-link voltage. For example, the 3L-T^{2}I following a three-level boost (TLB) converter [32] as shown in Fig. 1 can be used to apply the FT method in [26]–[28] with no output voltage degrading. Besides the conventional two-stage inverter, an impedance-source network can be used before the conventional multilevel inverter [29]–[31]. The configurations in [29]–[31] provide buck-boost operation in single-stage power conversion, allowing for the compensation of output voltage degradation in postfault operation by boosting the dc-link voltage. Especially, the work in [31] provides a full OCF solution for all active switches with smaller component voltage stress compared to that in [29] and [30].

The single-stage inverters in [29]–[31] require a very high dc-link voltage to generate a desired output voltage, which increases component voltage rating, especially for the upper and lower switches of the T-type circuit. Furthermore, the OCF and SCF that occurs at semiconductor devices of the impedance-source network are not considered in [29]–[31]. The conventional solution for OCF of upper or lower switch in [26] and [29]–[31] is not able to address the OCF of multiple upper or lower switches.

This article introduces some control techniques for TLB T-type inverter (TLB-T^{2}I) to solve existing drawbacks of solutions in [26]–[31]. The rest of this article consists of six sections. Sections II and III present PWM schemes for TLB-T^{2}I in normal and post-fault operation. Design guidelines and power loss calculations are included in Section IV. Some comparisons of component voltage stress between the proposed method and prior methods are shown in Section V. The experimental results and conclusion are attached in Sections VI and VII, respectively.

II. Operating of TLB-T^{2}I in Normal Condition

The configuration of TLB-T^{2}I shown in Fig. 2 consists of a boost network and a conventional 3L-T^{2}I, followed by a three-phase low-pass LC filter and output resistive load. The TLB circuit includes a boost inductor L_B, two capacitors C_P and C_N, two switches S_P and S_N, and four diodes $D_1 - D_4$. Compared to the conventional TLB shown in Fig. 1, this topology uses two more diodes, D_2 and D_3. These extra diodes help to immune shoot-through state in the inverter side circuit. As a result, this configuration can limit the SC current generated when SCF of the inverter side switch occurs. The 3L-T^{2}I ensures a three-level voltage at output pole voltage V_{XO} ($X = A, B, C$), which are denoted as states [P], [O], and [N]. The switching states of 3L-T^{2}I are like those of a conventional voltage-source inverter, which is given in Table I. In normal condition, the TLB-T^{2}I is introduced to work as a two-stage inverter. The dc-link voltage, V_{PN}, is controlled by two switches S_P and S_N. The interleaved control for both switches S_P and S_N to reduce inductor current ripple can be found in [33]. The capacitor voltages can be calculated as [33]

$$V_{CP} = V_{CN} = V_{\rm dc}/[2(1-D)] \quad (1)$$

TABLE I
on/off STATES OF 3L-T^{2}I ($X = A, B, C$)

State	ON Switch	V_{XO}
[P]	S_{1X}, S_{2X}	$+V_{PN}/2$
[O]	S_{2X}, S_{3X}	0
[N]	S_{3X}, S_{4X}	$-V_{PN}/2$

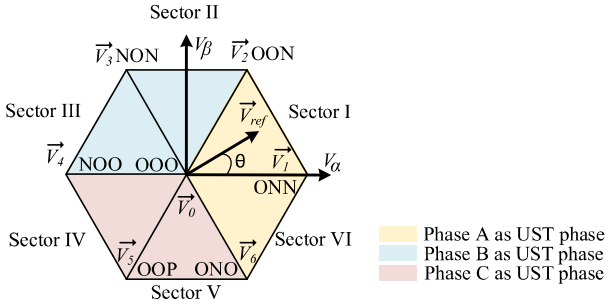

Fig. 3. Space vector diagram of proposed S_P OC FT method.

where D is the duty ratio of switches S_P and S_N ($D < 1$).

The inverter side is controlled by the conventional space vector modulation (SVM) method [34]. In this scheme, the peak-value of output phase voltage ($V_{x,\text{peak}}$) is expressed as

$$V_{x,\text{peak}} = 2/\sqrt{3}MV_{PN}/2 = 1/\sqrt{3}MV_{\text{dc}}/(1-D) \quad (2)$$

where M is modulation index ($M \leq 1$); V_{PN} is dc-link voltage.

The voltage gain, G, of the inverter is calculated as

$$G = V_{x,\text{peak}}/(V_{\text{dc}}/2) = 2/\sqrt{3} \times M/(1-D). \quad (3)$$

III. FAULT-TOLERANT METHODS FOR TLB-T^{2}I

A single OCF is considered in this section. The failure is divided into two cases: a failure of the boost side switch, and a failure of the inverter side switch. The OCFs at the inverter circuit are divided into two groups: the OCF at upper switch S_{1X} or lower switch S_{4X} ($X = A$, B, and C) and the OCF at bidirectional switches S_{2X} and S_{3X}. Because of symmetry, only OCF at S_P, OCFs at S_{1A} and bidirectional switch fault at S_{2A} and S_{3A} are considered.

A. FT for OCF at S_P

Assume that the OCF occurs at switch S_P. The capacitor C_N voltage is decreased while the capacitor C_P voltage is increased. The neutral voltage is unbalanced, which generates distortion at the output voltages. This OCF can be addressed by working as a two-stage two-level inverter with the modified space vector diagram shown in Fig. 3.

In proposed method, the inverter side produces two states at output voltage, V_{XO}, as [O] and [N]. State [O] denotes that V_{XO} is zero, which is generated by activating both switches S_{2X} and S_{3X}. While state [N] represents that V_{XO} is -V_{CN}, which is ensured by turning ON both S_{3X} and S_{4X}. In postfault operation, switch S_{3X} is always turned ON. The switching state combinations are shown in Fig. 3. The state [NNN] generated by activating switches S_{4A}, S_{4B}, and S_{4C} is not utilized.

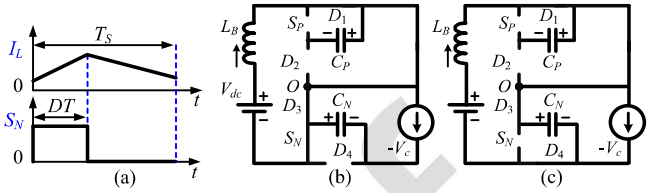

Fig. 4. (a) Control signals of switch S_N, and operating modes to tolerate S_P OCF. (b) Mode 1. (c) Mode 2.

In general, sector I is considered as an example for analysis. Three voltage vectors $\vec{V}_0$, $\vec{V}_1$, and $\vec{V}_2$ are adopted to generate reference vector $\vec{V}_{\text{ref}}$. The relationship between these voltage vectors is shown as

$$\begin{cases} \vec{V}_{\text{ref}}.T_s = \vec{V}_0.t_0 + \vec{V}_1.t_1 + \vec{V}_2.t_2 \\ T_s = t_0 + t_1 + t_2 \end{cases} \quad (4)$$

where T_s is the sampling period; and t_0, t_1, and t_2 are on-times of vectors $\vec{V}_0$, $\vec{V}_1$, and $\vec{V}_2$, respectively.

Vectors $\vec{V}_0$, $\vec{V}_1$, and $\vec{V}_2$ are defined as

$$\begin{cases} \vec{V}_{\text{ref}} = 1/\sqrt{3}.M.V_{CN}.e^{j\theta} \\ \vec{V}_0 = 0 \\ \vec{V}_1 = 2/3.V_{CN}.e^{j0} \\ \vec{V}_2 = 2/3.V_{CN}.e^{j\pi/3} \end{cases} . \quad (5)$$

By substituting (5) into (4), the dwell-times of these candidate voltage vectors can be identified as

$$\begin{cases} t_1 = MT_s \sin(\pi/3 - \theta) \\ t_2 = MT_s \sin(\theta) \\ t_0 = T_s - t_1 - t_2 \end{cases} . \quad (6)$$

The switching sequence of the sector I is [OOO]-[OON]-[ONN]-[OON]-[OOO]. In this sector, phase A always produces state [O] at the output side. Thus, to boost the C_N voltage, this method inserts the upper-shoot-through (UST) state into phase A to generate modes 1 and 2 shown in Fig. 4. In these modes, switches S_{1A}, S_{2A}, and S_{3A} are simultaneously turned ON, while diode D_2 is reverse-biased. Note that this insertion still generates state [O] at V_{AO}. The result is that capacitor C_P is disconnected from the main circuit, and two-level operation of the inverter is ensured by capacitor C_N.

The boost operation is ensured by controlling the duty cycle of switch S_N. The control signal of S_N is shown in Fig. 4(a). When switch S_N is turned ON, inductor L_B stores energy from the dc input source. When switch S_N is triggered OFF, the inductor voltage and input source charge for the capacitor C_N. The voltage across capacitor C_N can be calculated as

$$V_{CN} = V_{\text{dc}}/(1-D). \quad (7)$$

The C_N voltage is twice that in normal condition for the same duty ratio, D, which ensures desired amplitude of output voltage, as shown in (8). The voltage gain is kept as (3)

$$V_{x,\text{peak}} = 2/\sqrt{3} \times M \times V_{CN}/2 = 1/\sqrt{3} \times M \times V_{\text{dc}}/(1-D). \quad (8)$$

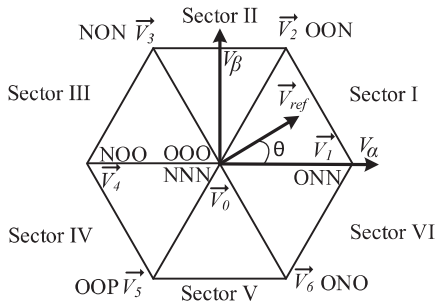

Fig. 5. Space vector diagram of proposed method for S_{1A} OC FT.

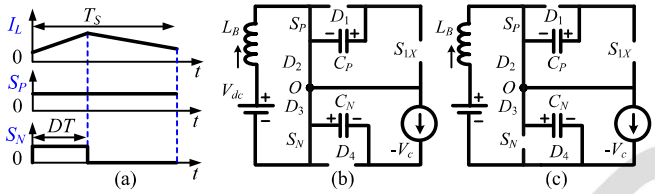

Fig. 6. (a) Control signals of switches S_P and S_N, and operating modes to tolerate S_{1A} OCF. (b) Mode 1. (c) Mode 2.

B. OCF at S_{1A}

Under OCF of S_{1A}, the output voltage V_{AO} cannot obtain the state [P]. This fault distorts the output voltage because the positive half cycle cannot be achieved. As a result, two capacitor voltages are seriously unbalanced. Similar to the OCF at S_P, the OCF at S_{1A} can be solved by applying a two-stage two-level control method. Under the proposed scheme, switch S_P is always triggered on, which reverses biased diode D_1, as shown in Fig. 6. Two states [O] and [N] at output pole voltage, V_{XO}, are generated by the same way as FT method for S_P OCF. Switches S_{1B} and S_{1C} are always triggered OFF in postfault operation of S_{1A} OCF. The operating of inverter side is the same as a conventional two-level inverter, which depends on the location of the reference vector $\vec{V}_{\text{ref}}$. For example, when the reference vector, as shown in Fig. 5, falls in sector I, the switching sequence is [OOO]-[OON]-[ONN]-[NNN]-[ONN]-[OON]-[OOO]. The dwell-time calculation is detailed in (4)–(6). Unlike FT method for the OCF at S_P, vector [NNN] is also used in the case of S_{1A} OCF. The boost operation is also achieved by adjusting the duty ratio D, of switch S_N, as shown in Fig. 6(a). The voltage across capacitor C_N and output voltage are also expressed as (7) and (8).

C. OCF at S_{2A} and S_{3A}

The OCF of S_{2A} and S_{3A} is not important when compared with OCF of S_P and S_{1A}. Output voltage V_{AO} cannot reach state [O] under S_{2A} and S_{3A} OCF conditions. This causes a slight total harmonic distortion (THD) increment at the output voltage and unbalanced capacitor voltages.

To solve this OCF, in sectors I–VI, the operation of the inverter can be guaranteed by using the redundant voltage vectors. For example, assuming that the reference vector is located in region 2 of sector I, as shown in Fig. 7. In normal condition,

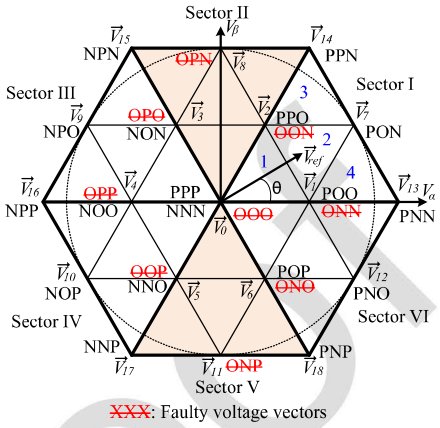

Fig. 7. Space vector diagram to solve bidirectional switch OCF.

the switching sequence is [PPO]-[POO]-[PON]-[OON]-[ONN] and return. When OCFs at S_{2A} and S_{3A} occur, vectors [OON] and [ONN] cannot be reached. Thus, small vectors [PPO] and [POO] are used, instead. This replacement does not affect the output voltage because the vectors [PPO] and [OON], [POO] and [ONN] generate the same output voltage. The switching sequence is [PPO]-[POO]-[PON] and return. The dwell-times of these vectors can be obtained by the same way as the conventional method [32].

In sectors II and V, medium vectors [OPN] and [ONP] cannot be reached in postfault operation. Unfortunately, these vectors do not have any redundant vectors. Therefore, the three-level operation is not ensured in sectors II and V. The FT method introduces two-level operation in sectors II and V. In detail, if the reference vector falls in sector II, three voltage vectors $\vec{V}_0$, $\vec{V}_{14}$, and $\vec{V}_{15}$ are utilized to synthesize the reference vector. It is worth noting that vectors [PPP] and [NNN] are used instead of zero vector [OOO]. The switching sequence for sector II is [PPP]-[PPN]-[NPN]-[NNN] and return. The dwell-time calculations for these vectors are expressed as

$$\begin{cases} t_{14} = MT_s \sin(2\pi/3 - \theta) \\ t_{15} = MT_s \sin(\theta - \pi/3) \\ t_0 = T_s - t_{14} - t_{15} \end{cases}. \tag{9}$$

In this method, the faulty phase is working as a two-level inverter while the healthy phase is still working as a three-level inverter.

D. OCF at D_1/D_4, SCF at D_2/D_3, and SCF at S_P/S_N

The OC-FT methods for OCFs of S_P/S_N, S_{1X}/S_{4X}, and S_{2X}/S_{3X} are the main contributions of this article. However, these three methods can cover some extra semiconductor failures. In OC-FT method for S_{1A}, switches S_{1B} and S_{1C} are always turned OFF. Hence, this control method can be extended to solve the OCF of S_{1A}, S_{1B}, and S_{1C} that occurs at the same time. This cannot do in the conventional methods [26]–[31]. Moreover, diodes D_1 and D_2 are always reverse biased and forward biased. Thus, this control scheme can be used to handle with the OCF of D_1 and the SCF of D_2. In this case, switch S_P is

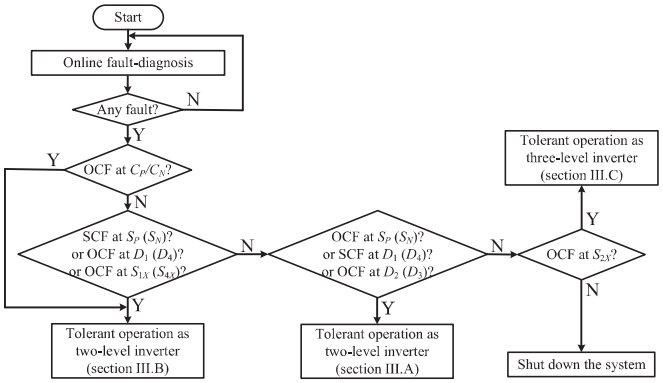

Fig. 8. Flowchart of FT operation of TLB-T^{2}I.

always gated on, thus, S_P SCF can be addressed by this control technique. Because of the symmetry of TLB-T^{2}I, the OCF at D_4, SCF at D_3 and S_N, can be solved by the same way.

E. OCF at D_2/D_3 and SCF at D_1/D_4

In FT method for S_P, diode D_2 is always reverse biased whereas D_1 is always forward biased. Thus, this PWM method can be applied to solve the OCF of D_2 and the SCF of D_1. The same way can be used to handle with OCF at D_3, and SCF at D_4, because of system symmetrical characteristic.

F. OCF/SCF at Upper/Lower Capacitors

Like switching devices, the capacitor is also able to face with OCF or SCF. The SCF at the capacitor usually causes a high SC current through the capacitor. It results in destroying this capacitor, and the SCF is changed to an OCF. It can be seen that the FT methods for S_P and S_{1A} OCFs do not use upper capacitor C_P. Therefore, both methods can be used to solve the OCF of capacitor C_P. The same way can be applied to handle with the OCF of capacitor C_N.

G. Flowchart of Fault-Tolerant Operation

The flowchart of FT operation of TLB-T^{2}I is shown in Fig. 8. An online diagnosis is adopted to monitor the system. The fault-diagnosis method in [9] can be applied for online fault-diagnosis function. If any fault is detected, it is addressed depending on type of fault. If the fault is OCF at C_P/C_N or SCF at S_P/S_N or OCF at D_1/D_4 or OCF of S_{1X}/S_{4X}, the FT method introduced in Section III.B is activated. If the fault is OCF at S_P/S_N or SCF at D_1/D_4 or OCF at D_2/D_3, the FT method introduced in Section III-A is utilized. If the fault occurs at bidirectional switch S_{2X}/S_{3X}, the FT method introduced in Section III-C is activated. The system is stopped when any another type of fault is detected.

IV. Design Guidelines and Power Loss Contribution

A. Design Guidelines

The component selection is presented to ensure the operation of the inverter in both normal and failure cases. When the inverter changes from normal to failure mode (S_P/S_{1A} OCFs), the component rating is obviously increased. Therefore, the inverter is designed to ensure the postfault operation of S_P/S_{1A} OCF. The voltage rating of all semiconductor devices and capacitors is maximized when applying FT methods for S_P/S_{1A} OCFs, which equals to the dc-link voltage, V_{PN}. Similarly, the current rating of all devices is maximized when applying S_P FT method, which is equal to the inductor current. Therefore, the semiconductor devices, inductor, and capacitors are selected to operate with dc-link voltage and input current. Under S_P/S_{1A} OCF, the boost circuit behaves as a conventional dc–dc boost converter. Therefore, the inductor and capacitor are selected like a conventional boost circuit as follows:

$$\begin{cases} L_B \geq V_{\rm dc} D T_S/(x\% I_L) \\ C_P = C_N \geq I_{PN} D(1-D) T_S/(y\% V_{\rm dc}) \end{cases} \quad (10)$$

where $x\%$ and $y\%$ are percentages of inductor current ripple and capacitor voltage ripple, T_S is the switching period.

TABLE II
Inverter Components

Components	Parameters
S_P/S_N and $S_{1X}-S_{4X}$	IMW120R020M1H (1200 V, 98 A, $r_{ds,on}$ = 19 mΩ)
D_1/D_4	IMW120R020M1H (1200 V, 60 A, V_F = 1.5 V)
D_2/D_3	VS-65EPS12LHM3 (1200 V, 65 A, V_F = 1.12 V)
L_B	3mH/50mΩ
C_P/C_N	2.2mH/50mΩ

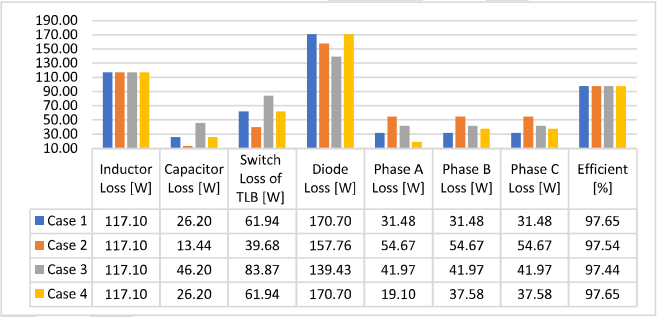

Fig. 9. Power loss analysis for the TLB-T^{2}I.

B. Power Loss Contribution

The power loss calculation for the TLB-T^{2}I is conducted in four cases as follows: case 1) normal condition, case 2) post-fault operation of S_P OCF, case 3) postfault operation of S_{1A} OCF, and case 4) postfault operation of S_{2A} and S_{3A} OCF. The system parameters used for power loss calculation are given in Table II. The inverter is designed to operate with 400 V input voltage, 220 $V_{\rm RMS}$/ 380 $V_{\rm RMS}$ three-phase output voltage, and 20 kVA. The dc-link voltage, V_{PN}, is boosted to 800 V. With the help of PSIM software, the power loss analysis of the inverter under the four cases mentioned above is obtained, as shown in Fig. 9. The inverter can obtain a high efficiency (97.65% for case 1) if it is carefully designed. With the help of new generation of semiconductor devices like SiC MOSFET/Diode, the performance of the inverter is not too much changed when it goes from normal

TABLE III
COMPARISON BETWEEN PROPOSED METHOD WITH OTHERS UNDER OC FAULT-TOLERANT

	Two-stage Inverter (Fig. 1)	3L-qZSI [29]	3L-qSBI [30]	3L-qSBI [31]	Proposed Method
Boost factor, B	$1/(1\text{-}D)$ for $F2$ and $F3$	$1/(1-2D)$ for $F2$ and $F3$	$1/(1-2D)$ for $F2$ and $F3$	$1/(1-2D)$ for $F1$ $2/(1-2D)$ for $F2$ and $F3$	$1/(1\text{-}D)$ for $F1$ and $F2$ and $F3$
Voltage gain, G	$M\times B/\sqrt{3}$ for $F2$ $2M\times B/\sqrt{3}$ for $F3$	$M\times B/\sqrt{3}$ for $F2$ $2M\times B/\sqrt{3}$ for $F3$	$M\times B/\sqrt{3}$ for $F2$ $2M\times B/\sqrt{3}$ for $F3$	$M\times B/\sqrt{3}$ for $F2$ $2M\times B/\sqrt{3}$ for $F1$ and $F3$	$2M\times B/\sqrt{3}$ for $F1$ and $F2$ and $F3$
Capacitor voltage stress, V_C/V_{dc}	$B/2$ for $F2$ and $F3$	$(1-D)B/2$ for $F2$ and $F3$	$B/2$ for $F2$ and $F3$	B for $F1$ $B/2$ for $F2$ and $F3$	$B/2$ for $F3$ B for $F1$ and $F2$
Diode voltage stress, V_D/V_{dc}	$B/2$ for $F2$ and $F3$	$B/2$ for $F2$ and $F3$	$B/2$ for $F2$ and $F3$	B for $F1$ $B/2$ for $F2$ and $F3$	$B/2$ for $F3$ B for $F1$ and $F2$
Switch S_P/ S_N voltage stress, V_S/V_{dc}	$B/2$ for $F2$ and $F3$	NA	$B/2$ for $F2$ and $F3$	B for $F1$ $B/2$ for $F2$ and $F3$	$B/2$ for $F3$ B for $F1$ and $F2$
Switch S_{4X} voltage stress, V_{S4X}/V_{dc}	B for $F2$ and $F3$	B for $F2$ and $F3$	B for $F2$ and $F3$	B for $F1$ and $F2$ and $F3$	B for $F1$ and $F2$ and $F3$
Capacitors	2	4	2	2	2
Diodes	2	2	2	4	4
Fault-tolerant	$F2$ and $F3$	$F2$ and $F3$	$F2$ and $F3$	$F1$ and $F2$ and $F3$	$F1$ and $F2$ and $F3$
Tolerate multiple OCF at S_{1X}/S_{4X}	No	No	No	No	Yes
Solving diode OCF/SCF	NA	NA	NA	OCF of D_2/D_3 SCF of D_1/D_4	OCF/SCF of D_1, D_2, D_3, D_4
Solving boost switch (S_P/S_N) OCF/SCF	NA	NA	NA	OCF	OCF & SCF
Solving capacitor OCF	NA	NA	NA	Yes	Yes

$F1$: S_P OCF $F2$: S_{1A} OCF $F3$: S_{2A} and S_{3A} OCFs NA: Not Applicable

operation to FT operation. For example, the efficiency of the inverter is only decreased by 0.21% when the S_{1A} FT method is activated and by 0.11% for the S_P FT method.

V. COMPARISON STUDY

In this section, the conventional control technique presented in [26] is considered to compare with the proposed method. Note that, in the FT method for half-bridge switch OCF, this method reduces the output voltage to half of that in normal condition. Therefore, in order to be fair, the conventional two-stage inverter shown in Fig. 1 is utilized to employ the method in [26]. In post faultoperation, the boost network produces more dc-link voltage to compensate for the degradation of output voltage. The other configurations, which are three-level quasi-Z-source inverter (3L-qZSI) in [29] and three-level quasi-switched boost inverter (3L-qSBI) in [30] and [31], are also considered in this comparison. In [29]–[31], the dc-link boost characteristic is ensured by the impedance-source network. The overall comparison is given in Table III. To put it simply, symbols $F1$, $F2$, and $F3$ are respectively used for OCFs of S_P, S_{1A}, and bidirectional switch S_{2A}/S_{3A}.

The qZS network in [29] uses the largest number of inductors and capacitors. The works in [30] and [31], two-stage inverter, and proposed method require smaller passive components than [29]. For the OCF at S_{1A}, the bidirectional switch of the faulty phase is always turned ON during post-fault condition and two healthy phases are used to recover output voltage, in [26], [29]–[31]. Thus, the works in [29]–[31] and two-stage inverter just solve a single OCF at one upper switch of the inverter branch (S_{1A}, or S_{1B}, or S_{1C}). While the proposed method turns OFF all upper switches when OCF occurs in one of these three switches. As a result, this scheme can be extended to solve multiple upper or lower switch OCFs, as given in Table III. Moreover, the proposed techniques can address many types of device failures of TLB circuit, which have not been mentioned in previous studies. Full OCFs/SCFs of switch S_P/S_N, and OCFs/SCFs of diodes $D_1 - D_4$ are not well discussed in [29]–[31], and two-stage inverter, while these failures can be solved by proposed methods. Furthermore, the OCF of capacitors C_P and C_N can be addressed by the proposed method and method in [31], which is not obtained in two-stage inverter and methods in [29] and [30]. There are two FT methods for OCF of the capacitor, whereas there is only one control technique for this failure in [31]. As a result, the proposed techniques are more flexible than the work in [31].

The comparison of voltage stress on devices in post-fault condition is shown in Fig. 10. To be simple, only the maximum value of voltage stress is mentioned in this comparison. For example, there are four capacitors in 3L-qZSI. However, only max value of capacitor voltages is considered in this work. Among these studies, the proposed method, conventional two-stage inverter, and method in [29] produce the smallest capacitor voltage rating for $F1$, $F2$, and $F3$ FT methods. This advantage can be achieved by using many capacitors in [29] and a large modulation index in the proposed scheme and a two-stage inverter.

The diode and switch voltage stresses are affected by the dc-link voltage. The dc-link voltage depends on the modulation index. In detail, the dc-link voltage can be calculated as follows:

$$V_{PN} = 2 \times V_{x,\text{peak}}/M. \tag{11}$$

In (11), the use of a larger modulation index produces a smaller dc-link voltage requirement, which causes reduction of voltage stress on diodes and switches, as shown in Fig. 10(b) and (c). The TLBT^{2}I with proposed method can operate at highest modulation index as the conventional two-stage inverter. As a result, it produces lower voltage ratings on diodes and switches than other works in [29]–[31]. Especially, in the $F2$ FT method, the proposed method uses only one capacitor C_N while the

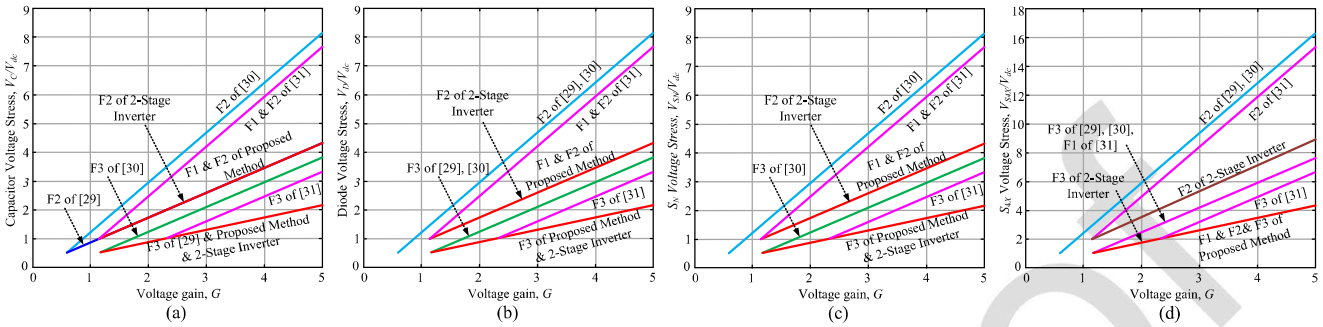

Fig. 10. Comparison between proposed method and others. (a) G vs. capacitor voltage stress. (b) G versus diode voltage stress. (c) G versus boost network switch voltage stress. (d) G versus S_{4X} switch voltage stress.

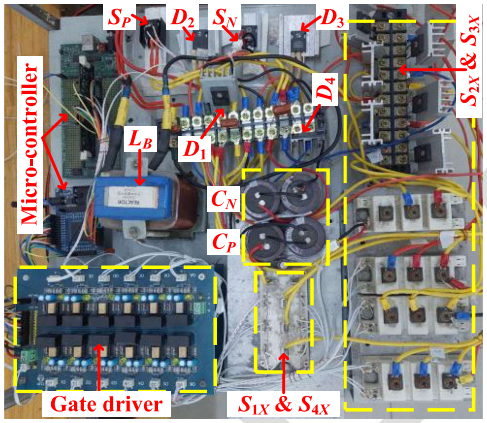

Fig. 11. Experimental prototype.

TABLE IV
EXPERIMENTAL PARAMETERS

Parameter/ Components		Values
DC input source	V_{dc}	200 V
AC output voltage	$V_{x,RMS}$	110 V_{RMS}
Line frequency	f_0	50 Hz
Switching frequency	f_s	10 kHz
Boost inductor	L_B	3 mH/20 A
Boost Capacitors	C_P and C_N	1 mF/800 V
Low-pass filter	L_f & C_f	3 mH and 10 µF
Resistor load	R_X	40Ω
Boost switches	S_P, S_N	60R060P7
Boost diodes	$D_1 - D_4$	VS-60APF12-M3
Upper/Lower switches	S_{1X}, S_{4X}	SKMGD123D
Bidirectional switches	S_{2X}, S_{3X}	SKM75GB12T4 and DSEI60-12A

conventional two-stage inverter uses both capacitors C_P and C_N. Thus, the proposed method can reduce the voltage rating of S_{4X} by 50% when compared to the conventional two-stage inverter, as shown in Fig. 10(d).

VI. EXPERIMENTAL RESULTS

A 1-kW laboratory prototype, shown in Fig. 11, has been built to verify the accuracy of the proposed methods. The T-type inverter is based on a six IGBTs SKMGD123D module, a SKM75GB12T4 modules and diodes DSEI60-12A. The TLB network is constructed by MOSFETs 60R060P7 and diodes VS-60APF12-M3. Because of the limitations of the laboratory, the optimal prototype cannot be obtained. The inverter and control parameters used in the experiment are given in Table IV. Note that only three main FT methods for S_P, S_{1A}, and bidirectional switch S_{2A} and S_{3A} OCFs are included in the experiment. The fault-detection method can be found in many studies like [8], [9]. In particular, the switch voltage can feedback to the microcontroller to detect semiconductor failure, quickly [9]. Therefore, this article just focuses on verifying the FT methods. Wang et al. [24], [25], the OCF is generated by cutting of the corresponding control signal. All the OCFs are assumed to appear at the beginning of phase A output voltage. The fault operation occurs during a single output period. The corresponding FT method is activated in the next output period.

The proposed methods have been tested at 200 V input voltage. In normal condition, the two capacitor voltages are boosted to 200 V, as shown in Figs. 12 –14 and Table V. Both capacitor voltages are balanced. Thus, the dc-link voltage V_{PN} achieves 400 V. The RMS value of output current is 2.66 A_{RMS}. The output current waveform is sinusoidal with the help of LC filter. The output pole voltage V_{XO} has three voltage levels: +200, 0, and -200 V. The FFT spectra of output line-to-line voltage is shown in Fig. 15. The THD of output line-to-line voltage V_{AB} is 49.4%, as given in Table V.

A. Results When S_P OCF

The experimental results when OCF occurs at S_P are presented in Fig. 12. During OCF of S_P, the drain-source of S_P is opened, whereas the lower switch S_N operates normally. It makes capacitor C_P voltage slightly increase, whereas lower capacitor C_N voltage is slightly decreased, as shown in Fig. 12(a). The output pole voltage and output load current have critical distortion, as illustrated in Fig. 12(b) and (c).

Under the proposed method, the UST of inverter side is activated, which causes capacitor C_P to be disconnected from the main circuit. Thus, the capacitor voltage V_{CP} keeps constant during post-fault condition, as shown in Fig. 12(a). In this time interval, the dc-link voltage is equal to C_N voltage. With 400 V of C_N voltage, the dc-link voltage is maintained as that in normal condition, which helps to recover the amplitude of output load current, as presented in Fig. 12(b). The output pole voltage V_{XO} has two voltage levels, which are 0 and -400 V, in

TABLE V
EXPERIMENTAL COMPARISON BETWEEN NORMAL AND FAULT CONDITIONS

	V_{CP}	V_{CN}	THD_{VAB}	Voltage rating, RMS current											
				S_P	S_N	D_1	D_2	D_3	D_4	S_{1A}	S_{2A}= S_{3A}	S_{4A}	S_{1B} = S_{1C}	S_{2B} = S_{3B} = S_{2C} = S_{3C}	S_{4B} = S_{4C}
Normal	200 V	200 V	49.4%	200 V 3.58 A	200 V 3.58 A	200 V 3.58 A	0 V 3.17 A	0 V 3.17 A	200 V 3.58 A	400 V 1.75 A	200 V 1.86 A	400 V 1.75 A	400 V 1.75 A	200 V 1.86 A	400 V 1.75 A
F1	200 V	400 V	96.3%	Fault	400 V 3.58 A	0 V 5.43 A	200 V 0 A	400 V 3.43 A	400 V 3.81 A	400 V 4.21 A	400 V 1.97 A	400 V 1.82 A	400 V 4.21 A	400 V 1.97 A	400 V 1.82 A
F2	0 V	400 V	99.8%	0 V 5.56 A	400 V 3.58 A	0 V 0 A	0 V 5.56 A	0 V 3.64 A	400 V 3.94 A	Fault	400 V 2.27 A	400 V 2.27 A	400 V 0 A	400 V 2.27 A	400 V 2.27 A
F3	200 V	200 V	66.7%	200 V 3.58 A	200 V 3.58 A	200 V 3.58 A	0 V 3.17 A	0 V 3.17 A	200 V 3.58 A	400 V 2.21 A	Fault	400 V 2.21 A	400 V 1.81 A	200 V 1.74 A	400 V 1.81 A

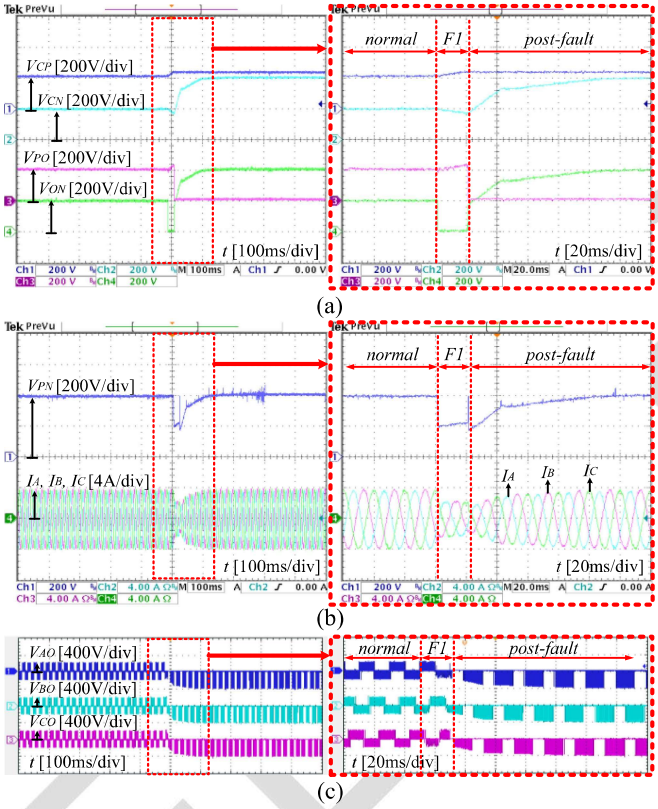

Fig. 12. Experimental results for S_P OC FT method.

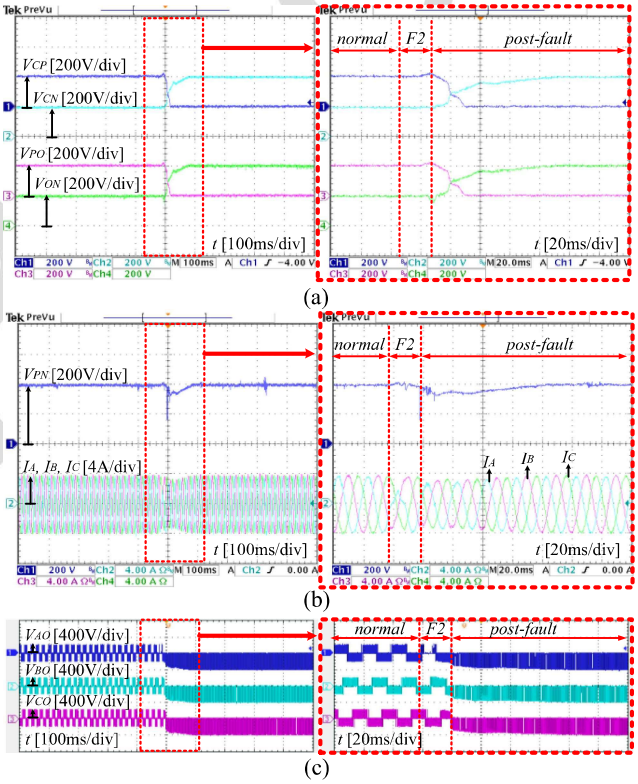

Fig. 13. Experimental results for S_{1A} OC FT method.

post-fault operation. Because the proposed method does not use the voltage vector [NNN], the output pole voltages are clamped to the dc-link mid-point in one-third of the output voltage period, as illustrated in Fig. 12(c). The FFT spectra of V_{AB} in postfault operation of S_P OCF is shown in Fig. 15(b). The THD of output line-to-line voltage V_{AB} is 96.3%, which is higher than that in normal condition because the inverter now operates with a two-level output voltage.

B. Results When S_{1A} OCF

Fig. 13 shows the experimental results for the S_{1A} OCF FT method. When OCF of switch S_{1A} occurs, the output voltage V_{AO} cannot achieve a value of +200 V, as shown in Fig. 13(c). It results in the distortion of phase A load current in the positive half cycle, as illustrated in Fig. 13(b). The distortion of phase A current also affects two healthy phase currents.

When activating the proposed method, the capacitor C_P voltage is discharged from 200 V to zero with the help of healthy upper switches, S_{1B} and S_{1C}. The capacitor C_N voltage is boosted to 400 V, as shown in Fig. 13(a). In steady-state, the dc-link voltage, V_{PN}, is equal to V_{ON}, because the upper capacitor voltage is zero. The dc-link voltage and output load currents are equal to that in normal condition. The FFT spectra of V_{AB} is shown in Fig. 15(c). The THD output line-to-line voltage is 99.8%, as presented in Table V.

C. Results When S_{2A} and S_{3A} OCFs

The experimental results for bidirectional switch OCF are presented in Fig. 14. Compared to the OCFs of S_P and S_{1A}, the OCFs of S_{2A} and S_{3A} generate less serious distortion in output currents. The proposed method, based on a modified SVM method, is applied to address this problem. As mentioned

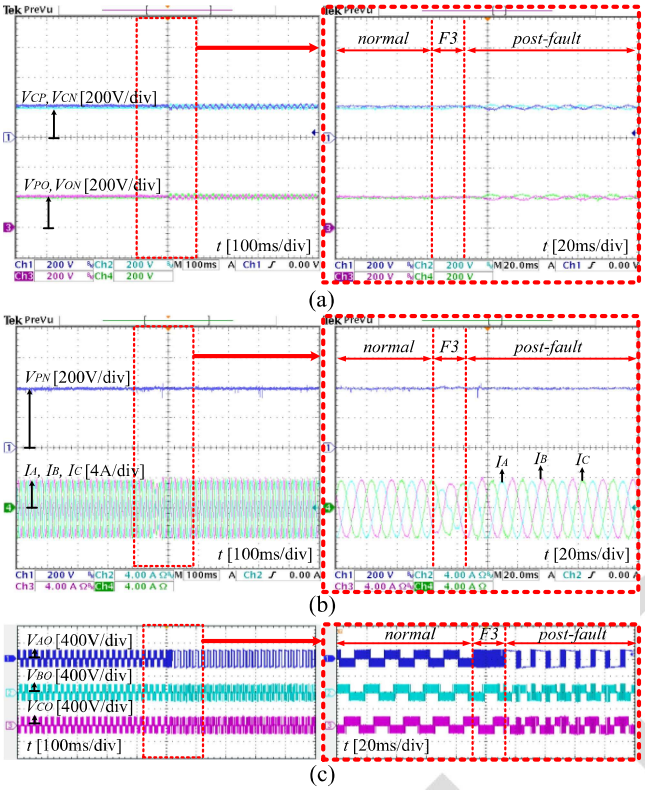

Fig. 14. Experimental results for bidirectional switch OC FT method.

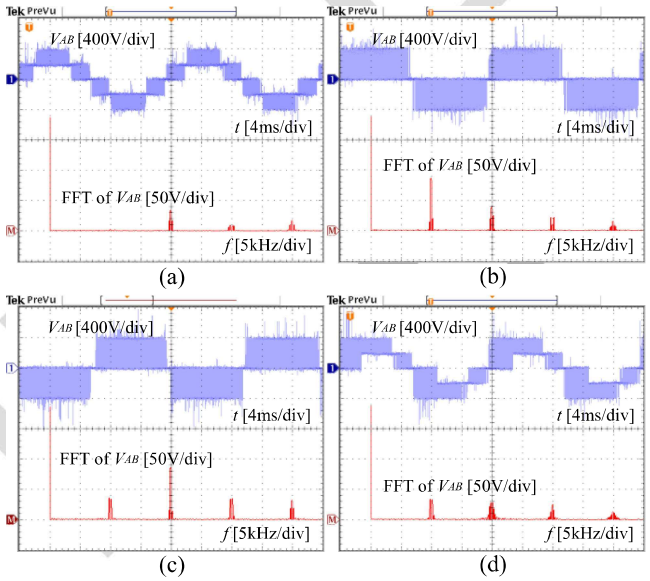

Fig. 15. FFT spectra of output line-to-line voltage under (a) normal condition and FT methods for (b) S_P OCF, (c) S_{1A} OCF, and (d) S_{2A} and S_{3A} OCFs.

in Section III-C, phase A is introduced to generate two-level output voltage, whereas the other healthy phases operate with three-voltage levels at output terminals, as shown in Fig. 14(c). At most times of the output period, phase A is clamped to positive/negative point of dc-link voltage. The amplitudes of dc-link

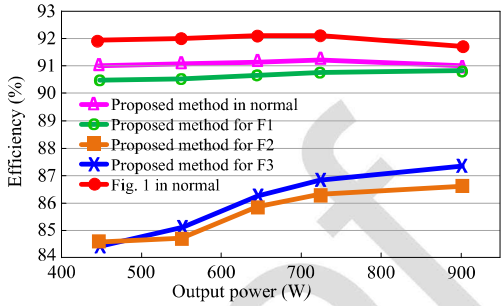

Fig. 16. Experimental efficiency.

voltage and output load current are equal to those in normal condition. This method causes a slight oscillation in capacitor voltages. However, these capacitor voltages are still balanced and do not have a critical effect to output current quality. The FFT spectra of V_{AB} is presented in Fig. 15(d). As given in Table V, the $F3$ FT method produces a smaller THD value at V_{AB} than the $F1$ and $F2$ FT methods, which is 66.7%. Except for $F2$, both FT methods for S_P and S_{1A} cause voltage and current rating increment.

D. Inverter Efficiency

The system efficiency under normal and failure modes of the proposed methods are presented in Fig. 16. The measured efficiency of the conventional topology in Fig. 1 in normal condition is also considered in this experiment. By adding two diodes (D_2 and D_3) to achieve FT capability, the efficiency of TLBT^{2}I is slightly lower (just 0.91% at 725-W) than the topology in Fig. 1. In FT methods for S_P fault ($F1$) and S_{1A} fault ($F2$), the switch voltage stress is increased, which leads to increase both switching and conduction losses. For example, the duty ratio of switch S_P will be increased when the inverter changes from normal to $F1$ mode, which generates more conduction loss of switch S_P. Moreover, the use of the UST insertion method for $F2$ FT is also the reason for the conduction loss increment. As a result, the system efficiencies in these cases are lower than in normal and bidirectional switch fault conditions.

VII. Conclusion

The full OCF of semiconductor devices as well as SCF at diodes/switches of TLB-T^{2}I was addressed with the introduced PWM methods. The voltage rating of devices like capacitors and semiconductors was improved compared to existing PWM methods, significantly. This benefit has been demonstrated through some comparison studies. Under the proposed method for upper or lower switch OCF, the voltage rating of inverter half-bridge switches was reduced at least to half of that in conventional methods. Moreover, the proposed methods can cover all diode and boost switch OCFs and SCFs. The failure of the capacitor was also addressed with the proposed methods. Thus, it was concluded that the system reliability was improved. The experiment was conducted to validate the accuracy of the introduced theory.

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An DPWM for Active DC-Link Type Quasi-Z-Source Inverter to Reduce Component Voltage Rating

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Abstract: The conventional DC-link type quasi-Z-source inverter has been known as a buck–boost inverter with a low component voltage rating. This paper proposes an active DC-link type quasi-Z-source inverter by adding one active switch and one diode to the impedance-source network to enhance the voltage gain of the inverter. As a result, the component voltage rating of the inverter is significantly reduced, which is demonstrated through some comparisons between the proposed topology and others. A discontinuous pulse width modulation (DPWM) scheme is proposed to control the inverter, which reduces the number of commutations compared to the traditional strategy. Under this approach, the insertion of a shoot-through state does not cause any extra commutations compared to the conventional voltage-source inverter. Details about control implementation, steady-state analysis, and design guidelines are also presented in this paper. Simulation and a laboratory prototype have been built to test the proposed inverter. Both buck and boost operations of the proposed inverter are implemented to validate the performance of the inverter.

Keywords: active quasi-Z-source inverter; DC-link type; discontinuous pulse width modulation; switching commutation reduction; impedance-source inverter

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1. Introduction

Presently, inverters that convert energy from a DC input source to AC output voltage play an important role in the renewable energy system. Because of their simple structure, low component utilization, and high power density, conventional two-level inverters are used in a wide range of industrial applications [1–4]. Two forms of traditional two-level inverters are voltage source inverters (VSI) and current source inverters (CSI). The VSI works as a voltage buck converter, where the peak-to-peak value of the AC output phase voltage is smaller than the DC link voltage. In comparison with VSI, the CSI is known as a boost converter, which uses many extra elements such as diodes [3]. Nowadays, inverters adopting a wide range of input voltage have attracted many researchers. However, conventional VSI and CSI do not adopt a wide range of input sources. In fact, the traditional solution installs a DC–DC boost converter in front of the conventional VSI to provide buck–boost characteristics in two-stage power conversion. In this way, the input voltage is enhanced before feeding to the inverter circuit. In this solution, a short-circuit current generated by activating all switches in one or more phase legs can destroy the system. This state is known as the shoot-through (ST) state and is forbidden in VSI. To avoid this dangerous situation, dead-time control is adopted to generate control signals for inverter switches [5,6]. In this case, the rising edge of the control signal is delayed to avoid the ST state. It causes distortion at output voltage and an increment in total harmonic distortion (THD) of output current. Many pulse-width modulation (PWM) methods based on the direction of output current have been explored to compensate for the negative effects of dead time [5,6]. However, these studies introduced more control complexity and required many additional current sensors.

In the last two decades, impedance source inverters (ISIs) (known as single-stage inverters) have been considered to solve the problems of buck–boost operation and the ST immunity of conventional VSI. The Z-source inverter (ZSI) is the first generation of ISIs, which was explored by Professor Peng in 2003 [7]. In ZSI, two capacitor voltages of the ZS network are subtracted by input voltage to produce the DC link voltage of the inverter side. Thus, it can be concluded that the capacitors are badly utilized. The quasi-Z-source inverter (qZSI) introduced a new connection type of impedance source network to overcome the limit of ZSI [8,9]. Two main types of qZSI are continuous qZSIs (CqZSI) and DC-link type/discontinuous qZSI (DqZSI). These two topologies have the same boost factor. However, the DqZSI topology has a smaller voltage rating of a capacitor than CqZSI, as presented in [8]. The main advantage of the CqZSI compared to DqZSI is that this topology has a continuous input current [8]. Many comparisons between ISIs and traditional two-stage inverters have demonstrated that single-stage inverters have better system reliability and output quality [10–12]. Moreover, when the voltage gain of the inverter is less than two, the ZSI and qZSI have higher efficiency than the conventional two-stage inverter [10,12]. The work in [13] introduced a combination of a qZS network and a single-phase neutral point clamped inverter for photovoltaic (PV) applications. With generic semiconductor devices, this work can obtain 97% conversion efficiency, just like any two-stage inverter. It demonstrated that the single-stage inverter is one of the promising topologies.

Two main issues of the impedance source inverter can be listed as (1) improving boost factor and voltage gain, and (2) reducing the number of switching commutations. When the boost factor/voltage gain is improved, the required ST duty ratio is also reduced. It results in reducing conduction loss and increasing system efficiency [14]. Moreover, the ST duty ratio also affects the inductor's current profile. Thus, a lower ST duty ratio causes a smaller inductor current ripple, which reduces the size of the inductor and increases the power density of the inverter. The switching commutation increment is mainly due to ST insertion. At least two extra commutations are generated for ST insertion in conventional methods for ISIs. It leads to increased switching losses of the semiconductor devices. Many studies have discussed switching commutation and ST duty ratio reductions, as follows.

The switching commutations can be minimized by correspondingly placing ST state, which is reported in [15–17]. Accordingly, the number of switching commutations is reduced to equal that of conventional VSI in [15–17]. Many studies have reported on voltage gain improvement methods for qZSI [18–22]. The first solution to increasing voltage gain is to add more extra passive components like inductors and diodes into the impedance-source network [18,19]. The other one is using active switches in the intermediate network [20–22]. In [18,19], one or more switched inductor (SL) units, which consist of two inductors and three diodes, are used to replace single inductors in the conventional topology of ZSI/qZSI to increase voltage gain. This solution increases the cost and size of the inverter because it utilizes many inductors. In comparison to the first solution in [18,19], the second one in [20–22] can save many inductors and diodes by using one extra active switch. It is worth noting that the boost factor and voltage gain of the topologies in [20–22] are very flexible to be controlled and higher than that in [18,19]. The work in [21] presented a combination of both solutions, which adopts both SL unit and active switch in the intermediate network. Although the voltage gain of these works has increased significantly, it remains low. Moreover, the boost factor is controlled by only the ST duty ratio, which makes the inverter inflexible.

This paper presents a new topology of active DC link type qZSI (ADC-qZSI) by adding one active switch and one diode into the conventional DqZSI. With the help of these extra devices, the proposed topology introduces one extra mode besides two conventional operating modes for ISIs (ST mode and non-ST mode). In this mode, the current of the inductor is kept constant and the voltage gain is increased. It results in component voltage rating reduction. A discontinuous PWM (DPWM) control method is proposed to control this topology. In this control technique, the ST state is inserted into the phase operating with the highest reference signals. It leads to reducing the number of switching commutations

down to equal to conventional two-level VSI. The next parts of this paper include seven sections. The inverter structure and steady-state analysis and design guidelines of the proposed inverter are presented in Sections 2 and 3, respectively. Section 4 presents the semiconductor loss calculation. The comparison study, simulation and experimental results are attached in Sections 5–7.

2. Proposed Active DC-Link Type Quasi-Z-Source Inverter (ADC-qZSI) Topology

Two types of proposed ADC-qZSIs have been drawn in Figure 1. Both types are constructed by an ADC-qZS network followed by a conventional two-level inverter. The impedance source network is known as the boost unit and is formed by two inductors (L_1 and L_2), two capacitors (C_1 and C_2), one active switch (S_0), and two diodes (D_1 and D_2). Compared to traditional DC-link qZSI in [8], the proposed inverter has one extra active switch, S_0, and one extra diode, D_2. This insertion makes this topology flexible to control and increases the boost factor and voltage gain of the inverter. The conventional two-level inverter is responsible for buck operation. With the corresponding control method, the proposed inverter can buck and boost the output voltage from a single DC source, V_{dc}. Each leg of the inverter side consists of two active switches, S_{1X} and S_{2X}, which ensures a two-level voltage at the output terminals, $+V_{PN}$ and zero. In general, two types of ADC-qZSIs have similar operations, thus, type 1 shown in Figure 1a is selected for analysis.

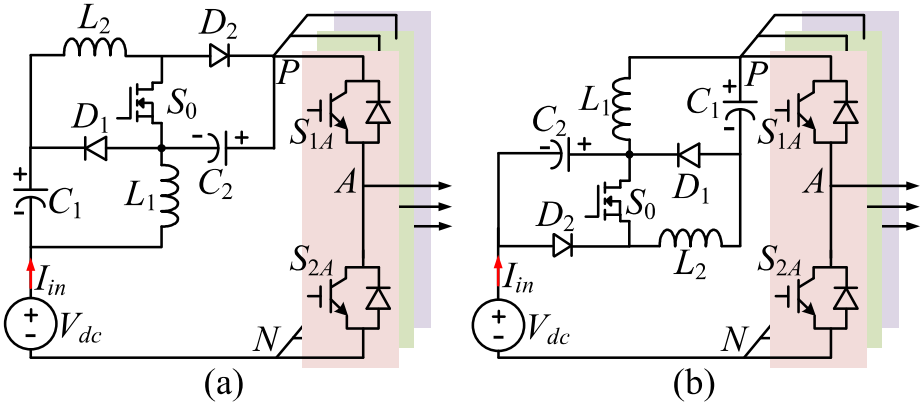

Figure 1. Topologies of ADC-qZSI: (**a**) Type 1 and (**b**) Type 2.

2.1. Operating States

Like any single-stage inverter, the ADC-qZSI is also proposed to operate under ST mode and non-ST mode, as shown in Figure 2. The on/off states of inverter switches and diodes are listed in Table 1.

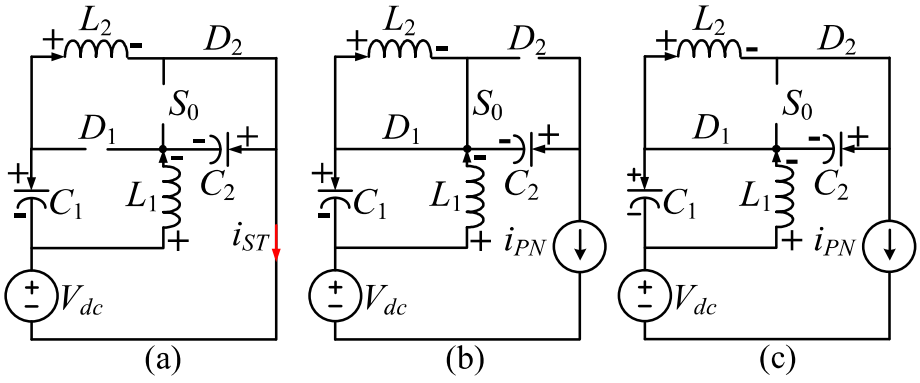

Figure 2. Operating modes of ADC-qZSI. (**a**) ST mode, (**b**) non-ST mode 1, (**c**) non-ST mode 2.

Table 1. On/Off states of ADC-qZSI (X = A, B, C).

Mode	ON Switch	ON Diode	V_{XN}
ST	S_{1X}, S_{2X}	D_2	0
non-ST 1	S_0, S_{1X}/S_{2X}	D_1	$+V_{PN}$, 0
non-ST 2	S_{1X}/S_{2X}	D_1, D_2	$+V_{PN}$, 0

In the ST state, as shown in Figure 2a, the inverter side is able to produce value of 0 V at three-phase output voltages by turning on two switches in one phase leg, while switch S_0 is gated off. As a result, the DC-link voltage, V_{PN}, is shorted and has a value of zero. This ST state reverses diode D_1 and forward diode D_2 of impedance source circuit. In this mode, inductor L_1 is stored energy from DC input voltage and capacitor C_2, while inductor L_2 is stored energy from DC input voltage and capacitor C_1. The inductor voltages and capacitor currents are expressed as follows:

$$\begin{cases} L_1 \frac{di_{L1}}{dt} = V_{dc} + V_{C2}; & L_2 \frac{di_{L2}}{dt} = V_{dc} + V_{C1} \\ C_1 \frac{dv_{C1}}{dt} = -i_{L2}; & C_2 \frac{dv_{C2}}{dt} = -i_{L1} \end{cases} \quad (1)$$

where V_{dc} is DC input source; V_{C1} and V_{C2} are capacitor C_1 and C_2 voltages; i_{L1}, i_{L2}, and i_{PN} are instantaneous values of inductor currents and equivalent inverter side current.

In non-ST mode, the DC-link voltage obtains maximum value, which is determined by the summing DC input source and two capacitor voltages. With one extra switch, S_0, the non-ST mode consists of two sub-modes depending on the state of S_0. When S_0 is gated on, non-ST mode 1 shown in Figure 2b is achieved. Diode D_2 is reversed bias, whereas diode D_1 is forward bias. It results in shorting inductor L_2 and discharging capacitor C_2. While capacitor C_1 is charged from inductor L_1. The following equations are obtained:

$$\begin{cases} L_1 \frac{di_{L1}}{dt} = -V_{C1}; L_2 \frac{di_{L2}}{dt} = 0 \\ C_1 \frac{dv_{C1}}{dt} = i_{L1} - i_{PN}; C_2 \frac{dv_{C2}}{dt} = -i_{PN} \end{cases} \quad (2)$$

It can be seen that this non-ST mode maintains the energy of inductor L_2 instead of discharging like conventional ISI, which increases the boost factor of the inverter.

Non-ST mode 2 of the proposed inverter, as shown in Figure 2c, is like any single-stage inverter. Switch S_0 is gated off, whereas the inverter side switches operate like conventional inverters. Two inductors transfer energy to capacitors. The following equations are achieved:

$$\begin{cases} L_1 \frac{di_{L1}}{dt} = -V_{C1}; & L_2 \frac{di_{L2}}{dt} = -V_{C2} \\ C_1 \frac{dv_{C1}}{dt} = i_{L1} - i_{PN}; & C_2 \frac{dv_{C2}}{dt} = i_{L2} - i_{PN} \end{cases} \quad (3)$$

2.2. Proposed DPWM Control Strategy

To reduce the switching commutation, the proposed method uses a DPWM strategy to generate the control signals to inverter switches. To detail this modulation method, let us first define three signals v_X (X = A, B, and C) as follows:

$$\begin{cases} v_A = 1/\sqrt{3} \times M \times \sin(2\pi f_o t) \\ v_B = 1/\sqrt{3} \times M \times \sin(2\pi f_o t - 2\pi/3) \\ v_B = 1/\sqrt{3} \times M \times \sin(2\pi f_o t - 2\pi/3) \\ M \leq 1 \end{cases} \quad (4)$$

where M is modulation index; f_o is fundamental frequency.

Three reference signals v_X^* (X = A, B, C), as shown in Figure 3, can be obtained by subtracting v_X from minimum value of v_A, v_B, v_C as follow:

$$v_X^* = v_X - \min(v_A, v_B, v_C) \quad (5)$$

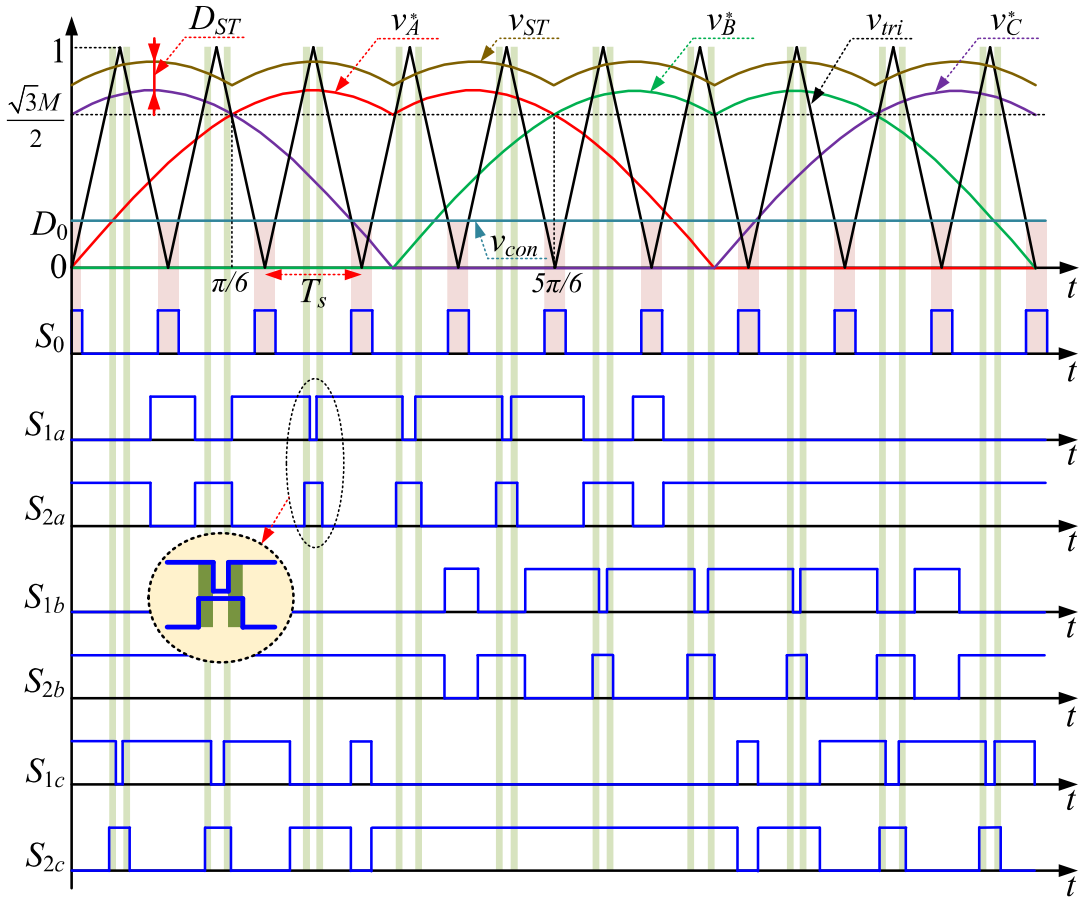

Figure 3. Proposed DPWM for introduced inverter.

These three reference signals are compared to high-frequency carrier V_{tri} like a conventional two-level inverter, to produce on/off switching signals for inverter side switches. In this scheme, one-third of the output period has no switching commutation in any phase leg, as shown in Figure 3. Thus, the switching loss can be reduced when compared to the conventional sinusoidal PWM method.

In the conventional PWM control method for single-stage inverters, the constant signal is used to generate the ST signal of the inverter leg. When this ST signal is inserted into the switching sequence, it produces at least two extra commutations in any phase leg. To overcome this, the proposed method uses discontinuous modulation signal v_{ST} and the maximum value of v_X^* to produce ST signal, as presented in Figure 3. In more detail, the ST signal is activated when $\max(v_A^*, v_B^*, v_C^*) \leq V_{tri} \leq v_{ST}$. Then, this ST signal is inserted into the phase which has the maximum value of reference signal v_X^* by triggering on both switches S_{1X} and S_{2X} of that phase leg. In this way, the ST insertion does not generate any extra switching commutation compared to conventional two-level VSI. For example, as shown in zoom-in waveforms of switches S_{1A} and S_{2A} control signals, there are only two switching commutations for each switch, which equals the conventional two-level inverter.

Like any impedance source two-level inverter, the ST state must be inserted within zero vectors. Therefore, ST duty ratio D_{ST} is not larger than $(1 - M)$ and can be controlled independently by M. The v_{ST} signal and ST duty ratio are expressed as follows:

$$\begin{cases} v_{ST} = \max(v_A^*, v_B^*, v_C^*) + D_{ST} \\ D_{ST} \leq 1 - M \end{cases} \tag{6}$$

where D_{ST} is ST duty ratio.

The control signal of S_0 is generated by comparing control signal v_{con} to carrier signal V_{tri}, as shown in Figure 3. The v_{con} is identified as:

$$v_{con} = D_0 \tag{7}$$

where D_0 is duty ratio of switch S_0.

In order not to affect the operating modes of the inverter, v_{con} must be satisfied with the following term:

$$v_{con} \leq \sqrt{3}M/2 \Leftrightarrow D_0 \leq \sqrt{3}M/2 \tag{8}$$

2.3. Steady-State Analysis

Figure 4 shows the profiles of inductor currents and capacitor voltages under one switching period, T_s. It is clear that the total time of ST mode is $D_{ST}{\cdot}T_s$ for any period T_s. The time interval of non-ST mode 1 is equal to the on-time of switch S_0 which is determined as $D_0{\cdot}T_s$. The rest time of T_s is $(1 - D_{ST} - D_0){\cdot}T_s$, which is the time interval of non-ST mode 2. By applying the volt-second balanced principle to two inductors, L_1 and L_2, the capacitor and DC link voltages can be identified as:

$$\begin{cases} V_{C1} = V_{dc}(1 - D_0)D_{ST}/(1 - D_0 - 2D_{ST} + D_0D_{ST}) \\ V_{C2} = V_{dc}D_{ST}/(1 - D_0 - 2D_{ST} + D_0D_{ST}) \\ V_{PN} = V_{dc}(1 - D_0)/(1 - D_0 - 2D_{ST} + D_0D_{ST}) \end{cases} \tag{9}$$

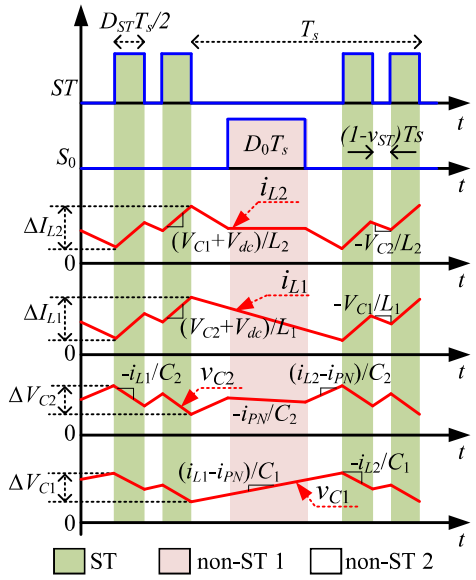

Figure 4. Inductor currents and capacitor voltages in one switching period.

Assuming that the equivalent inverter current, i_{PN}, is constant, the average values of inductor currents can be approximately calculated by applying capacitor charge-balanced principle to capacitor C_1 and C_2 currents, as follows:

$$\begin{cases} I_{L1} = i_{PN}(1 - D_0)(1 - D_{ST})/(1 - D_0 - 2D_{ST} + D_0D_{ST}) \\ I_{L2} = i_{PN}(1 - D_{ST})/(1 - D_0 - 2D_{ST} + D_0D_{ST}) \end{cases} \tag{10}$$

The boost factor, B, of the inverter is identified as:

$$B = \frac{V_{PN}}{V_{dc}} = \frac{1 - D_0}{1 - D_0 - 2D_{ST} + D_0D_{ST}} \tag{11}$$

The peak value of fundamental component of output phase voltage is calculated as:

$$\hat{v}_X = 1/\sqrt{3} \times M \times V_{PN} \tag{12}$$

where $\hat{v}_X$ is the peak value of output phase voltage.

The voltage gain, G, of proposed inverter is expressed as:

$$G = \frac{\hat{v}_X}{V_{dc}/2} = \frac{2}{\sqrt{3}} \times \frac{M \times (1 - D_0)}{1 - D_0 - 2D_{ST} + D_0 D_{ST}} \tag{13}$$

By setting D_0 to max value which is expressed in (8), the max voltage gain can be obtained.

3. Parameter Selection

3.1. Inductor and Capacitor Selection

As shown in Figure 4, the inductor current ripples are depended on the time interval of non-ST mode 2, $(1 - v_{ST})T_s$. When v_{ST} is maximum, the inductor current ripple is maximum. Based on (4)–(6), the maximum value of v_{ST} can be calculated as:

$$v_{ST,\max} = M + D_{ST} \tag{14}$$

Based on (1)–(3) and (14), the maximum value of inductor current ripples can be expressed as:

$$\begin{cases} \Delta I_{L1} = V_{dc} M(1 - D_0)/(KL_1 f_s) \\ \Delta I_{L2} = V_{dc} D_{ST}(M - D_0)/(KL_2 f_s) \\ K = 1 - D_0 - 2D_{ST} + D_0 D_{ST} \end{cases} \tag{15}$$

where ΔI_{Lj} (j = 1, 2) is inductor L_j current ripple; $f_s = 1/T_s$ is switching frequency.

The capacitor voltage ripples are calculated as:

$$\begin{cases} \Delta V_{C1} = i_{PN} M D_{ST}/(KC_1 f_s) \\ \Delta V_{C2} = i_{PN}[MD_{ST} - (K - D_{ST})D_0]/(KC_2 f_s) \end{cases} \tag{16}$$

Based on (9), (10), (15) and (16), the inductors and capacitors are selected in terms of $\Delta I_{Lj}/I_{Lj} \leq k_1\%$, and $\Delta V_{Cj}/V_{Cj} \leq k_2\%$, where $k_1\%$ and $k_2\%$ are max acceptable ratios of inductor current and capacitor voltage ripples, respectively.

3.2. Semiconductor Device Selection

The maximum reversed voltage of diode D_1 is DC-link voltage, which is obtained in ST mode. The max reversed voltage of diode D_2 equals the capacitor C_2 voltage, which is achieved in non-ST mode 1.

The maximum value of diode D_2 current is equal to the maximum value of inductor L_2 current, which is obtained in non-ST mode 2, while the current through diode D_1 achieves its maximum value in non-ST modes, which is calculated as:

$$\begin{cases} i_{D1,\max} = i_{L1,\max} + i_{L2,\max} - i_{PN} \\ i_{Lj,\max} = I_{Lj} + \Delta I_{Lj}/2 \text{ where } j = 1, 2 \end{cases} \tag{17}$$

where $i_{Lj,\max}$ is the maximum value of inductor L_j current, which can be calculated by applying (10) and (15).

Switch S_0 is only installed to transfer the energy of inductor L_2, and its current is constant when it is turned on, as shown in Figure 4. Thus, its current is the average value of the inductor L_2 current, which is expressed in (10). As shown in (9), the voltage across S_0 equals the voltage across capacitor C_2.

The voltage across the inverter side switches is equal to the DC link voltage. The maximum current through switch S_{1X} is ST current, which is determined by summing two max values of two-inductor currents.

4. Semiconductor Loss Contribution

The power loss of semiconductor devices is classified into two groups: (1) loss of semiconductor devices of an impedance source circuit, and (2) power loss of inverter side switches. MOSFET devices are adopted for switching devices in this analysis.

4.1. Loss of Switching Devices of Impedance-Source Network

As shown in Figure 3, the S_0 switch of the intermediate circuit has one switching action per switching period, T_S. The switching voltage and current of switch S_0 are capacitor C_2 voltage and inductor L_2 current, respectively. When S_0 is gated on, the current across S_0 is I_{L2} and the time interval of this state is D_0T_s. Therefore, the power loss of switch S_0 is calculated as:

$$\begin{cases} P_{S0,cond} = r_{ds,on} \times D_0 \times I_{L2} \\ P_{S0,sw} = \frac{1}{2} V_{C2} \times I_{L2} \times \left(t_{ri} + t_{fu} + t_{ru} + t_{fu} \right) \times f_s \end{cases} \quad (18)$$

where $P_{S0,cond}$ and $P_{S0,sw}$ are conduction and switching losses of S_0; t_{ri}, t_{fu}, t_{ru} and t_{fu} are respectively current rise time, current fall time, voltage rise time, and voltage fall time of MOSFET.

In any switching cycle, diode D_1 has two switching events when the ST state is activated. When diode D_1 is reverse biased, it blocks DC link voltage. When D_1 is forward biased, it transfers inductor L_1 current in non-ST mode two and two inductor currents in non-ST mode one. The conduction loss and reverse recovery loss of diode D_1 are expressed as:

$$\begin{cases} P_{D1,cond} = V_F \times (1 - D_{ST}) \times I_{L1} + V_F \times D_0 \times I_{L2} \\ P_{D1,rr} = 2 \times V_{PN} \times Q_{rr} \times f_s \end{cases} \quad (19)$$

where $P_{D1,cond}$ and $P_{D1,rr}$ are conduction and reverse recovery losses of D_1; V_F and Q_{rr} are forward voltage and reverse recovery charge of diode, respectively.

Diode D_2 has one switching action per switching cycle when the S_0 switch is turned on. The reverse voltage of diode D_2 is the capacitor C_2 voltage. When diode D_2 is forward biased in ST mode and non-ST mode two, it transfers inductor L_2 current. The power loss of this diode is calculated as follows:

$$\begin{cases} P_{D2,cond} = V_F \times (1 - D_0) \times I_{L1} \\ P_{D2,rr} = V_{C2} \times Q_{rr} \times f_s \end{cases} \quad (20)$$

4.2. Loss of Switching Devices of Inverter Side Circuit

Three phase legs of the inverter side circuit have the same operating principle. Therefore, only the S_{1A} and S_{2A} switches of the phase A leg are considered in this analysis.

From $\pi/6$ to $5\pi/6$ of output voltage, the reference signal v_A^* of phase A is the maximum. Thus, the ST state is inserted into this phase. This insertion makes S_{2A} switch at two-inductor currents. Similar to switch $S_{2A,}$ the switching current of switch S_{1A} is the sum of two-inductor currents and phase A load current. From 0 to $\pi/6$ and $5\pi/6$ to π, switch S_{1A} is switched at phase A load current. When switch S_{1A} is gated on, there is one reverse recovery action generated at the anti-parallel diode of switch S_{2A}. From π to $7\pi/6$ and $11\pi/6$ to 2π, switch S_{2A} is switched at phase A load current while there is one switching event of the body-diode of switch S_{1A}. Switches S_{1A} and S_{2A} have no switching action in the time interval from $7\pi/6$ to $11\pi/6$. Both switches S_{1A} and S_{2A} block DC link voltage like any conventional two-level VSI. The switching losses of both S_{1A} and S_{2A} are expressed as follows:

$$\begin{cases} P_{S1A,sw} & = \frac{2}{2\pi}\int_{0}^{\pi/6}\frac{1}{2}V_{PN}i_A(\theta)\left(t_{ri}+t_{fu}+t_{ru}+t_{fu}\right)f_s d\theta \\ & +\frac{1}{2\pi}\int_{\pi/6}^{5\pi/6}\frac{1}{2}V_{PN}[I_{L1}+I_{L2}+i_A(\theta)]\left(t_{ri}+t_{fu}+t_{ru}+t_{fu}\right)f_s d\theta+\frac{2}{2\pi}\int_{\pi}^{7\pi/6}V_{PN}Q_{rr}f_s d\theta \\ P_{S2A,sw} & = \frac{2}{2\pi}\int_{0}^{\pi/6}V_{PN}Q_{rr}f_s d\theta+\frac{1}{2\pi}\int_{\pi/6}^{5\pi/6}\frac{1}{2}V_{PN}(I_{L1}+I_{L2})\left(t_{ri}+t_{fu}+t_{ru}+t_{fu}\right)f_s d\theta \\ & +\frac{2}{2\pi}\int_{\pi}^{7\pi/6}\frac{1}{2}V_{PN}|i_A(\theta)|\left(t_{ri}+t_{fu}+t_{ru}+t_{fu}\right)f_s d\theta \end{cases} \quad (21)$$

where $P_{S1A,sw}$ and $P_{S2A,sw}$ are switching losses of switches S_{1A} and S_{2A}, respectively.

The conduction losses of switches S_{1A} and S_{2A} are expressed as:

$$\begin{cases} P_{S1A,cond} & = \frac{1}{2\pi}\int_{5\pi/6}^{13\pi/6}r_{ds,on}i_A^2(\theta)v_a^*(\theta)(d\theta \\ & +\frac{1}{2\pi}\int_{\pi/6}^{5\pi/6}r_{ds,on}\left\{i_A^2(\theta)v_a^*(\theta)+[i_A(\theta)+I_{L1}+I_{L2}]^2D_{ST}\right\}d\theta \\ P_{S2A,cond} & = \frac{1}{2\pi}\int_{5\pi/6}^{13\pi/6}r_{ds,on}i_A^2(\theta)[1-v_a^*(\theta)](d\theta \\ & +\frac{1}{2\pi}\int_{\pi/6}^{5\pi/6}r_{ds,on}\left\{i_A^2(\theta)[1-v_a^*(\theta)]+[I_{L1}+I_{L2}]^2D_{ST}\right\}d\theta \end{cases} \quad (22)$$

where $P_{S1A,cond}$ and $P_{S2A,cond}$ are conduction losses of switches S_{1A} and S_{2A}, respectively.

4.3. Power Loss Comparison between Proposed Topology and Conventional DqZSI

The proposed ADC-qZSI is compared to conventional DqZSI in [8] for semiconductor loss. In this comparison, two inverters are designed to operate under 200 V DC input source, 220 V_{RMS}/380 V_{RMS} AC output voltage, and 1.5 kW. The semiconductor components and operating parameters are listed in Table 2. With these parameters, the proposed topology needs 620-V DC-link voltage to generate 220 V_{RMS} AC output voltage. While it is 910 V DC-link voltage for conventional DqZSI. As a result, the proposed topology used 1200 V switching devices instead of 1700 V devices such as the conventional topology in [8]. In the proposed configuration, the voltage stresses of switch S_0 and diode D_2 are capacitor C_2 voltage, which is 340 V. Thus, switch S_0 and diode D_2 are 650 V switching devices. The result of the power loss comparison is shown in Figure 5. The proposed ADC-qZSI introduces two more power losses at S_0 and diode D_2 compared to the traditional DqZSI. However, the other semiconductor losses of the proposed topology are smaller than DqZSI because of having a smaller DC link voltage. As a result, the total semiconductor loss of introduced ADC-qZSI is smaller than the conventional DqZSI.

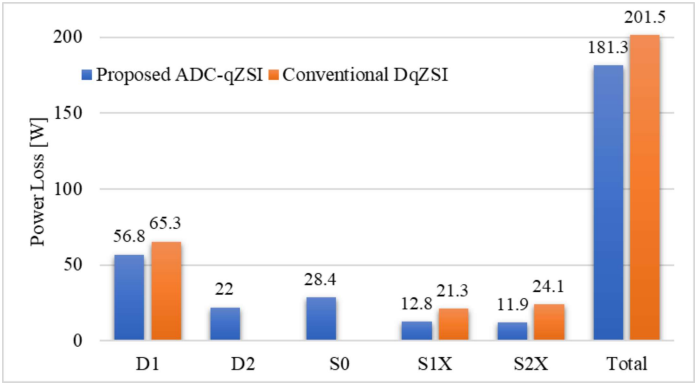

Figure 5. Comparison of semiconductor loss of proposed topology and conventional DqZSI in [8].

Table 2. Semiconductor and operating parameters.

Component	Proposed ADC-qZSI	Conventional DqZSI [8]
Switch S_0	IMZA65R030M1H (650 V, $r_{ds,on}$ = 30 mΩ)	NA
Switches S_{1X} and S_{2X}	IMZ120R030M1H (1200 V, $r_{ds,on}$ = 30 mΩ)	C2M0080170P (1700 V, $r_{ds,on}$ = 80 mΩ)
Diode D_1	GD2X30MPS12D (1200 V, V_F = 1.5 V)	GB50MPS17 (1700 V, V_F = 1.5 V)
Diode D_2	AIDW40S65C5 (650 V, V_F = 1.5 V)	NA
Modulation index, M	0.86	0.61
ST duty ratio, D_{ST}	0.14	0.39
Extra duty ratio, D_0	0.74	NA
Switching frequency, f_s	50 kHz	50 kHz

5. Comparison Study

The main contributions of the proposed configuration can be listed as (1) using a small number of passive components, (2) high voltage gain, and (3) low component voltage rating, which are verified by comparing to some previous single-stage inverters such as conventional DqZSI in [8], SL-qZSI in [18], rSL-qZSI in [19], ASC-EqZSI in [20], ASC/SL-qZSI in [21], and HG-qSBI in [22]. The comparison study concludes three sub-sections, which are (1) the number of components comparison; (2) boost factor and voltage gain comparison, and (3) component voltage stress comparison. Note that the proposed ADC-qZSI has two coefficients (D_0 and D_{ST}) to control the boost factor. Their relationship is shown in (6) and (8). Thus, in this comparison study, both maximum boost and minimum boost control are considered. In detail, the maximum boost control can be obtained by setting the value $\sqrt{3}(1 - D_{ST})/2$ for D_0, and the minimum boost control can be achieved by setting the zero value for D_0. It is worth noting that the ST duty ratios, D_{ST}, of these works are set as $(1 - M)$.

5.1. Number of Components

The overall comparison between these configurations has been summarized in Table 3. Among these topologies, the conventional DqZSI topology in [8] uses the smallest number of elements compared to others. However, it makes conventional topology have lower voltage gain and higher voltage stress compared to others, which is detailed in the next section. The SL-qZSI in [18] and rSL-qZSI in [19] do not use active switching devices in impedance source networks. Instead, they use more inductors and diodes to enhance voltage gain. In detail, the SL-qZSI in [18] uses one more inductor and two more diodes, while the rSL-qZSI in [19] uses two-more inductors and five more diodes compared to the proposed ADC-qZSI. The use of active switches in intermediate network topologies like [20–22] and the proposed topology helps save a large number of passive components like inductors and capacitors. The work in [21] uses two fewer inductors, one fewer capacitor, and two fewer diodes than in [19]. However, it still utilizes three more diodes than the proposed ADC-qZSI. Moreover, the use of only one capacitor [21] causes high capacitor voltage stress, which is detailed in the next part of this section. The proposed topology has the same number of components as ASC-EqZSI in [20] and HG-qSBI in [22], which are two inductors, two capacitors, two diodes, and only one active semiconductor device in the impedance-source network. Note that the inverter sides of these configurations use a conventional two-level inverter, thus, the number of elements for the inverter side circuit is the same for all these topologies.

Table 3. Overall Comparison Between Proposed Inverter and Other Single-Stage Inverters.

	DqZSI [8]	**SL-qZSI [18]**	**rSL-qZSI [19]**	**ASC-EqZSI [20]**	**ASC/SL-qZSI [21]**	**HG-qSBI [22]**	**Proposed ADC-qZSI**
Boost factor, B	$\frac{1}{1-2D_{ST}}$	$\frac{1+D_{ST}}{1-2D_{ST}-D_{ST}^2}$	$\frac{1+D_{ST}}{1-3D_{ST}}$	$\frac{1}{1-3D_{ST}+D_{ST}^2}$	$\frac{1+D_{ST}}{1-3D_{ST}}$	$\frac{1}{1-4D_{ST}+D_{ST}^2}$	$\frac{1-D_0}{1-D_0-2D_{ST}+D_0D_{ST}}$
Voltage gain, G	1.15·MB	1.15·MB	1.15·MB	1.15·MB	1.15·MB	1.15·MB	1.15·MB
Capacitor voltage stress, V_c/V_{dc}	$D_{ST}B, C_1$&C_2	$\frac{2D_{ST}}{1+D_{ST}}B, C_1$ $\frac{1-D_{ST}}{1+D_{ST}}B, C_2$	$\frac{2D_{ST}}{1+D_{ST}}B, C_1$ $\frac{1-D_{ST}}{1+D_{ST}}B, C_2$	$(1-D_{ST})B, C_1$ B, C_2	B	$D_{ST}B, C_1$ $(1-D_{ST})B, C_2$	$D_{ST}B, C_1$ $\frac{D_{ST}}{1-D_0}B, C_2$
Diode voltage stress, V_D/V_{dc}	B	B, D_{in} $\frac{1-D_{ST}}{1+D_{ST}}B, D_1$ $\frac{D_{ST}}{1+D_{ST}}B, D_{2\div3}$	B, D_{in} $\frac{D_{ST}}{1+D_{ST}}B, D_{1\div4}$ $\frac{1-D_{ST}}{1+D_{ST}}B, D_{5\div6}$	B, D_0 $(2-D_{ST})B, D_1$	B, D_{in} $\frac{D_{ST}}{1+D_{ST}}B, D_{1\div2}$ $\frac{2-2D_{ST}}{1+D_{ST}}B, D_3$	B, D_1 $(1-D_{ST})B, D_2$	B, D_1 $\frac{D_{ST}}{1-D_0}B, D_2$
Switch voltage stress, V_S/V_{dc}	NA	NA	NA	$(1-D_{ST})B$	B	$(1-D_{ST})B$	$D_{ST}/(1-D_0)B$
Inductors	2	3	4	2	2	2	2
Capacitors	2	2	2	2	1	2	2
Diodes	1	4	7	2	5	2	2
Impedance Switches	0	NA	NA	1	1	1	1
Common ground	Yes	Yes	Yes	Yes	No	No	Yes

5.2. Boost Factor and Voltage Gain

The boost factor and voltage gain of these topologies are shown in Figure 6. According to some studies [18–22], the HG-qSBI in [22] has the largest boost factor, as presented in Figure 6a, thus it also has the largest voltage gain. When the minimum boost control is applied, the boost factor of the proposed inverter is $1/(1-2D_{ST})$, which is equal to conventional qZSI in [8]. As a result, the proposed topology produces the smallest boost factor and voltage gain compared to the works in [18–22]. However, the boost factor of the proposed ADC-qZSI can be extended by increasing the duty ratio D_0 of switch S_0. When the duty ratio D_0 obtains a value of 0.5, the boost factor and voltage gain of the proposed method are equal to HG-qSBI in [22] and also higher than the works in [18–21]. When the maximum value of D_0, $\sqrt{3}(1-D_{ST})/2$, is achieved, the boost factor and voltage gain of the proposed ADC-qZSI are the largest, which brings a benefit to the low component voltage rating, as follows.

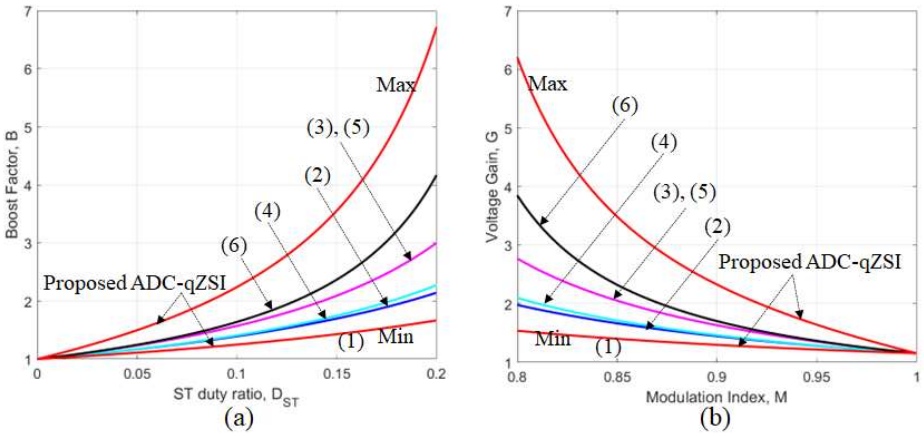

Figure 6. Comparison of boost factor and voltage gain: (**a**) ST duty ratio vs. boost factor, (**b**) modulation index vs. voltage gain. (1) DqZSI [8], (2) SL-qZSI [18], (3) rSL-qZSI [19], (4) ASC-EqZSI [20], (5) ASC/SL-qZSI [21], (6) HG-qSBI [22].

5.3. Component Voltage Rating

Some investigations on capacitor, diode and switch voltage stresses have been conducted, as illustrated in Figure 7. Note that there are a lot of diodes in these topologies, which have unequal voltage stresses, as shown in Table 3. Therefore, simply, the maximum values of diode voltage stresses are only considered in this comparison study. Figure 7a,b show voltage stress comparisons for capacitors C_1 and C_2. The max boost control of the proposed ADC-qZSI produces the smallest capacitors C_1 and C_2 voltage rating compared to others, as shown in Figure 7a,b. Among these topologies, the impedance-source switch voltage stress is equal to the capacitor voltage. Thus, having a lower capacitor voltage rating causes a lower switch voltage rating, as shown in Figure 7c.

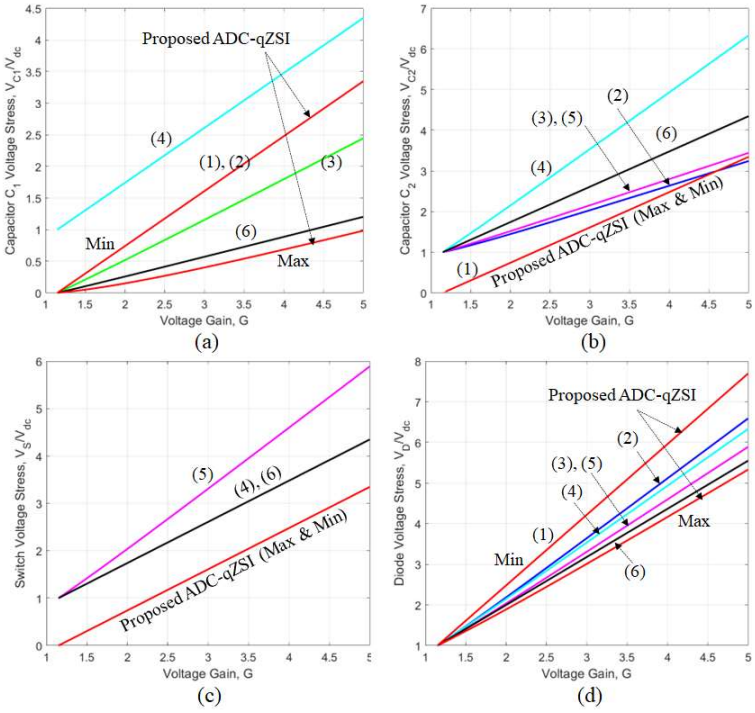

Figure 7. Comparison of component voltage rating: (**a**,**b**) voltage gain vs. capacitor voltage rating, (**c**) voltage gain vs. switch voltage rating, (**d**) voltage gain vs. diode voltage rating. (1) DqZSI [8], (2) SL-qZSI [18], (3) rSL-qZSI [19], (4) ASC-EqZSI [20], (5) ASC/SL-qZSI [21], (6) HG-qSBI [22].

Having a higher voltage gain makes the proposed ADC-qZSI able to use a higher modulation index compared to other topologies, as shown in Figure 6b. On the other hand, the boost factor can be calculated as follows:

$$B = G/(1.15 \times M) \tag{23}$$

From (23), it can be seen that the proposed topology with the introduced DPWM method uses a higher modulation index, which leads to requiring a lower boost factor. The max value of diode voltage stress equals the boost factor, as shown in Table 3. Moreover, it is clear that the inverter side switch voltage rating is also equal to the boost factor. As a result, the proposed ADC-qZSI has the lowest diode and inverter side switch voltage stresses among these configurations, as presented in Figure 7d.

6. Simulation and Experimental Verifications

6.1. Simulation Results

The boost operation of the proposed ADC-qZSI has been tested in this section. Both 56 Ω resistive load and 45 Ω–100 mH resistive–inductive load are installed at the output of the inverter for testing. The parameters used in the simulation are listed in Table 4. The

inverter is fed by a 150 V DC input voltage which is used to generate 110 V_{RMS} AC output load voltage. The modulation index M, ST duty ratio D_{ST}, and extra duty ratio D_0 are 0.81, 0.19, and 0.5, respectively. With these controlling parameters, two capacitor voltages, V_{C1} and V_{C2} are boosted to 66 V and 132 V for both loads, as shown in Figure 8. As a result, the peak value of DC-link voltage V_{PN} is 350V, approximately. For resistive load, two inductor currents, I_{L1} and I_{L2}, are continuous, and their values are 4.85 A and 9.57 A, respectively. While they are 3.96 A and 7.83 A because the real power of 45 Ω–100 mH resistive-inductive load is smaller than 56 Ω resistive load for the same 110 V_{RMS} AC output voltage. The output line-to-line voltage has three voltage levels, which vary from $-V_{PN}$ to $+V_{PN}$. The output load current amplitudes of these loads are the same which is 2.06 A_{RMS}. However, the current of the resistive-inductive load is a 30-degree lag compared to the current othe f resistive load.

Table 4. Simulation and experimental parameters.

Parameter/Components		Values
Input voltage	V_{dc}	150 V–400 V
AC output voltage	$V_{x,RMS}$	110 V_{RMS}
Output frequency	f_0	50 Hz
Switching frequency	f_s	10 kHz
Boost inductor	L_1, L_2	3 mH/20 A
Boost capacitors	C_1 and C_2	1 mF/400 V
LC filter	L_f and C_f	3 mH and 10 µF

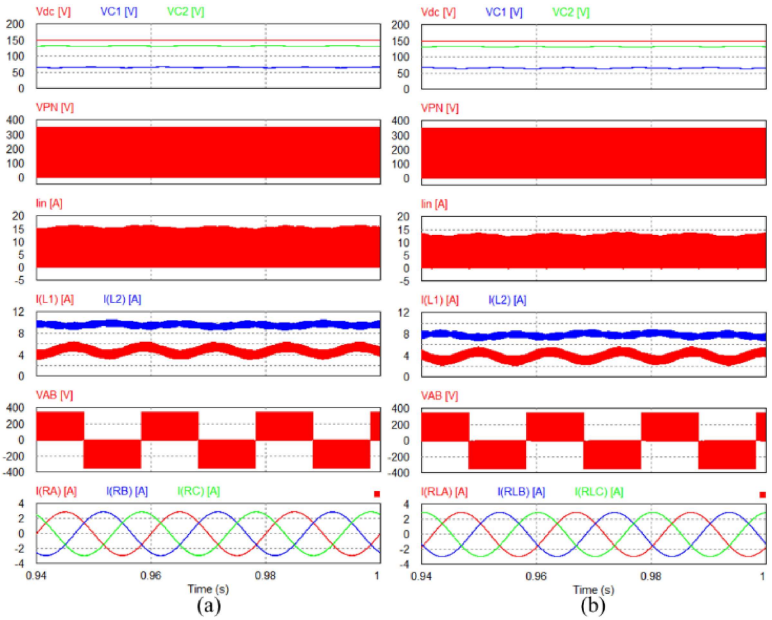

Figure 8. Simulation results for proposed ADC-qZSI under 150 V input voltage. (**a**) 56 Ω resistive load, (**b**) 45 Ω–100 mH resistive-inductive load.

6.2. Experimental Results

A laboratory prototype based on DSP TMS320F28335 has been built to verify the operation of the proposed inverter, as shown in Figure 9. Module six IGBTs SKMGD123D is utilized for the inverter-side circuit. Impedance source network is based on MOSFET 60R060P7, diode VS-60APF12-M3, 1 mF capacitors, and 3 mH inductors. A 56 Ω three-phase output resistive load is considered to test the proposed inverter, which is fed through the tLC filter (3 mH and 10 µF) to mitigate the high-frequency component of the output

voltage. The system parameters are listed in Table 4. The proposed ADC-qZSI is verified under buck and boost modes with the range of input DC voltage from 150 V to 400 V. In both cases, the parameters of the inverter are selected to generate 110 V_{rms} at the output load voltage, in theory.

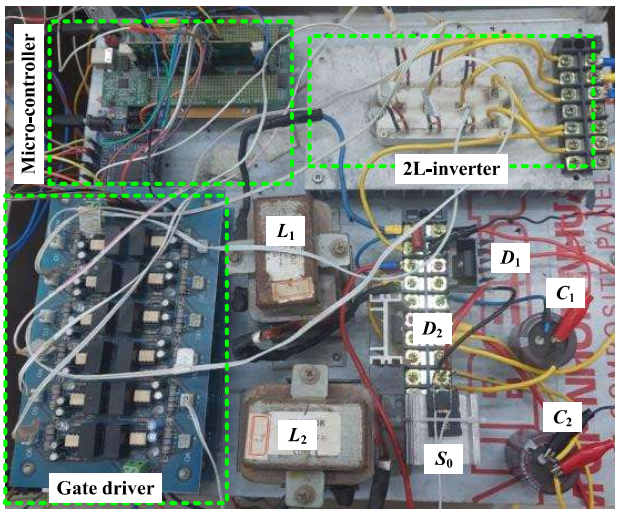

Figure 9. Experimental Prototype.

Firstly, a 150-volt input source is applied to test the inverter in boost mode. The experimental results for the 150-volt input voltage are shown in Figure 10. The impedance source network is utilized to boost the DC-link voltage, V_{PN}. In this case, the ST duty ratio D_{ST}, S_0 duty ratio, D_0 and modulation index, M are set as 0.19, 0.5 and 0.81, respectively. With these parameters, the voltages of two capacitors, V_{C1} and V_{C2} are boosted to 55 V and 105 V, respectively, as shown in Figure 10a. It results in 310 V of the peak value of DC-link voltage, V_{PN}, and output line-to-line voltage, V_{AB}, as shown in Figure 10b. As shown in Figure 10a,b, the input current is discontinuous and has an average value of 4.03 A, whereas the two inductor currents, I_{L1} and I_{L2}, are continuous and have average values of 4.08 A and 8.85 A, respectively. The zoom-in waveforms of two inductor currents, switch S_0 drain-source voltage and DC-link voltage are shown in Figure 10c. It shows that two inductor currents are increased linearly in the ST state, which is represented by the zero value of DC link voltage. When S_0 is turned on, the inductor L_2 current is kept constant. The voltage stress of S_0 is equal to the capacitor C_2 voltage. The output load voltage and current waveforms are sinusoidal because of using an LC filter. The RMS values of output load voltage and current are 104 V_{RMS} and 1.84 A_{RMS}.

In buck mode, a 400-volt DC input source is applied to test the inverter, the results are shown in Figure 11. The ST duty ratio D_{ST}, S_0 duty ratio, D_0 and modulation index, M are set as 0, 0.5 and 0.68, respectively. The input voltage is now high enough to produce 110 V_{RMS} at output load voltage. Therefore, two capacitor voltages are kept at 0 V, approximately, as illustrated in Figure 11a. The DC link voltage is equal to the input voltage. It also results in a 400-volt peak value of output line-to-line voltage, V_{AB}, as shown in Figure 11b. The waveforms of two inductor currents, switch S_0 drain-source voltage and DC-link voltage are shown in Figure 11c. The voltage stress of S_0 is 40 V, whereas the average values of two inductor L_1 and L_2 currents are 1.43 A and 1.94 A. The DC link voltage is equal to the input voltage. RMS values of output load voltage and current are 109 V_{RMS} and 1.92 A_{RMS}, respectively.

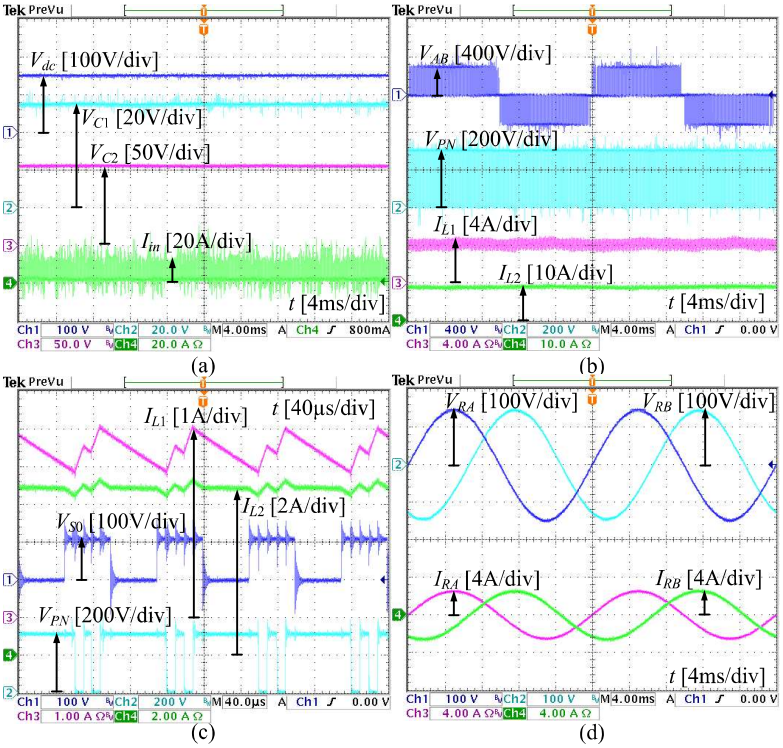

Figure 10. Experimental results for 150 V input voltage. From top to bottom: (**a**) input voltage V_{dc}, capacitor voltages V_{C1}, V_{C2}, input current I_{in}, (**b**) output line-to-line voltage V_{AB}, DC-link voltage V_{PN}, inductor currents I_{L1}, I_{L2}, (**c**) inductor currents I_{L1}, I_{L2}, switch S_0 voltage V_{S0}, DC-link voltage V_{PN}, (**d**) output load voltages and currents V_{RA}, V_{RB}, I_{RA}, I_{RB}.

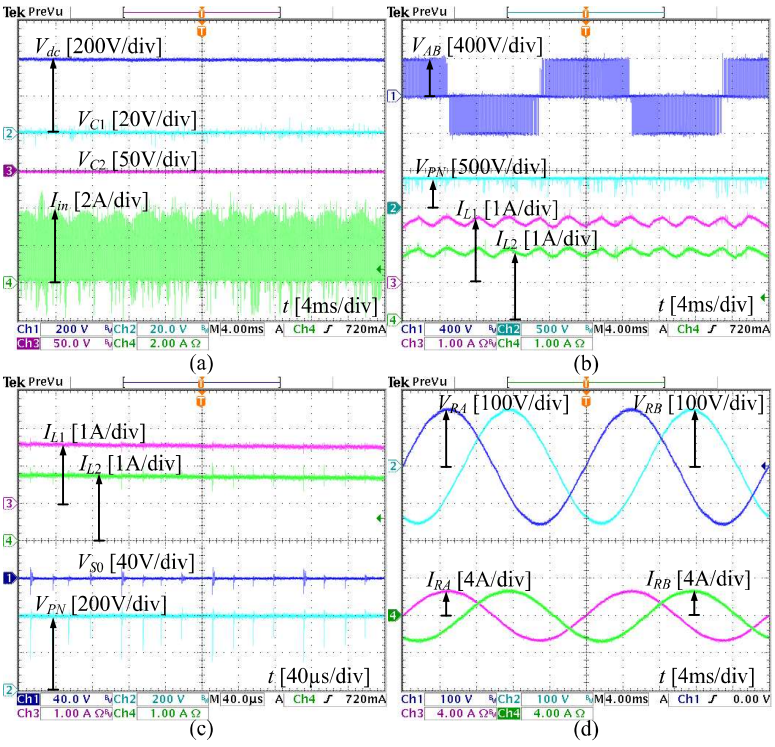

Figure 11. Experimental results for 400 V input voltage. From top to bottom: (**a**) input voltage V_{dc}, capacitor voltages V_{C1}, V_{C2}, input current I_{in}, (**b**) output line-to-line voltage V_{AB}, DC-link voltage V_{PN}, inductor currents I_{L1}, I_{L2}, (**c**) inductor currents I_{L1}, I_{L2}, switch S_0 voltage V_{S0}, DC-link voltage V_{PN}, (**d**) output load voltages and currents V_{RA}, V_{RB}, I_{RA}, I_{RB}.

Figure 12 shows the experimental results of the proposed inverter under variation of load in two cases: (1) the three-phase load change from 72 Ω to 40 Ω, and (2) the three-phase load change from 40 Ω to 72 Ω. Both cases cause a small effect on capacitor voltages and output load voltages. It is clear that the 40 Ω load causes higher load and device currents than the 72 Ω load. It results in more device loss for case one than for case two, which reduces capacitor voltages, as shown in Figure 12.

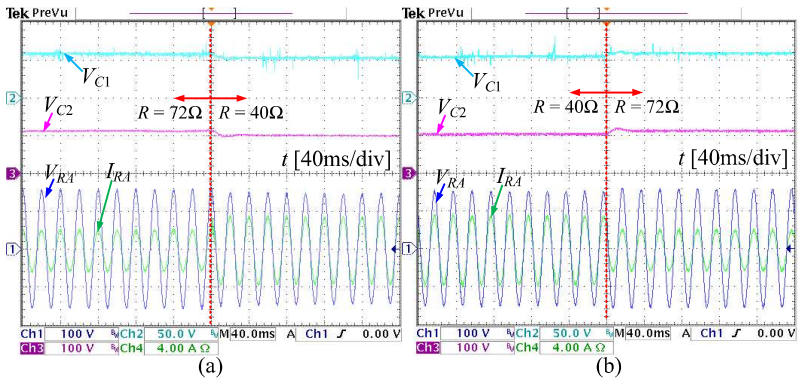

Figure 12. Experimental results under variation of load: (**a**) 72 Ω to 40 Ω, (**b**) 40 Ω to 72 Ω.

7. Conclusions

This paper proposed a new topology of ADC-qZSI by adding one active switch and one diode into the impedance source network. With these devices, one more operating mode is introduced for the proposed inverter besides the conventional ST and non-ST modes. During this extra mode, one inductor voltage is shorted. As a result, the energy of this inductor is maintained, which helps to increase the boost factor and voltage gain of the inverter compared to previous studies of single-stage inverters. Having higher voltage gain leads to the lower voltage rating of capacitors and switching devices. A DPWM control strategy reducing the number of commutations is presented to control this proposed inverter. Under this PWM method, the ST state insertion does not generate any extra commutations and the total switching commutations of the inverter are equal to conventional two-level VSI. Some comparisons between the proposed inverter and other previous single-stage inverters have been conducted to demonstrate these advantages. The simulation and experimental results have been presented to verify the operation of the proposed inverter. Both buck and boost modes are considered to test the inverter.

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Conflicts of Interest: The authors declare no conflict of interest.

Nomenclature

V_{dc}	DC input voltage
V_{C1}, V_{C2}	Capacitor C_1 and C_2 voltages
V_{PN}	DC-link voltage
V_{AB}, V_{RA}	Output line-to-line and load voltage
v_a, v_b, v_c	reference signals
v_{ST}	ST reference signal
I_{L1}, I_{L2}	Inductor L_1 and L_2 currents
ΔV_{C1}, ΔV_{C2}	Capacitor C_1 and C_2 voltage ripples
ΔI_{L1}, ΔI_{L2}	Inductor L_1 and L_2 current ripples
I_{RX}	Output load current of resistor R_X
I_{PN}	Equivalent inverter side current
I_{Dj}	Diode j current
M	Modulation index
D_{ST}	ST duty ratio
D_0	Switch S_0 duty ratio
f_0	Line frequency
f_s, T_s	Switching frequency and switching period
B, G	Boost factor and voltage gain
k_1%, k_2%	Percentage of current and voltage ripples
$P_{Sy,cond}$, $P_{S0,sw}$	Conduction and switching losses of switch S_y
$P_{Dj,cond}$, $P_{Dj,rr}$	Conduction and reverse recovery losses of diode Dj

Abbreviations

VSI, CSI	Voltage source inverter, current source inverter
ST	Shoot-through
THD	Total harmonic distortion
PWM	Pulse width modulation
DPWM	Discontinuous PWM
ISI	Impedance-source inverter
ZS, ZSI	Z-source, and Z-source inverter
qZSI	Quasi-Z-source inverter
CqZSI, DqZSI	Continuous qZSI, discontinuous/DC-link qZSI
PV	Photovoltaic
SL	Switched-inductor
ADC-qZSI	Active quasi-Z-source inverter
ASC-EqZSI	Active switched-capacitor-embedded qZSI
HG-qSBI	High gain quasi-switched boost inverter

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Space Vector Modulation Method-Based Common Mode Voltage Reduction for Active Impedance-Source T-Type Inverter

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ABSTRACT In recent years, many pulse width modulation techniques have been explored for three-level impedance-source inverters. Among them, a space vector modulation (SVM) technique using upper/lower shoot-through (UST/LST) insertion provides high voltage gain and satisfactory output voltage quality. This paper further introduces a new SVM control method to reduce the magnitude of common-mode voltage (CMV) without affecting the output voltage quality and voltage gain. With this approach, only small vectors with low magnitudes of CMV are adopted to synthesize an output voltage vector. The UST and LST states are also inserted to these small vectors to boost the DC-link voltage in high voltage gain and high modulation index. The comparison of CMVs between this strategy and other schemes is presented to demonstrate the effectiveness of the proposed method. The simulation and experiments are conducted to verify the accuracy of the theory.

INDEX TERMS Common-mode voltage reduction, quasi-switched boost inverter, three-level T-type inverter, space vector modulation.

I. INTRODUCTION

Conventional three-level T-type inverters (3L-T^{2}Is) have a simple structure and low conduction loss. They do not require many diodes or capacitors compared with other traditional configurations, such as three-level neutral-point-clamped inverters (3LNPCIs) or flying capacitor inverters. Because of these advantages, this topology provides superior low-voltage and medium-voltage applications, such as renewable energy systems or AC motor drives [1]–[3]. Nevertheless, this structure only provides a voltage buck capability, which is difficult to use in many applications requiring highly preferred AC output voltage from a low DC input power supply. To overcome this, two typical solutions were considered. The first one is to add a DC/DC boost converter to enhance the DC-link voltage before it is fed to the 3L-T^{2}I [4]. The second is to use a low-frequency AC/AC transformer behind the inverter to achieve the desired AC output voltage. Furthermore, during operation, the conventional 3L-T^{2}I does not accept the shoot-through (ST) state, which is generated when all switches in one or more phase legs are simultaneously turned on [5]. This limitation can be resolved by applying a dead time for control signals before the switches are turned on. However, this approach can cause distortion at the output voltage [6].

Because of the foregoing problems, a Z-source inverter (ZSI) was introduced [7]. With one additional diode, two inductors, and two capacitors, the ZSI is known as a single-stage inverter with buck–boost capability and ST immunity. By placing the ZS network between the DC input source and two-level inverter, the ST state boosts the DC-link voltage without affecting output voltage and system reliability. However, this topology of an impedance-source network also has certain disadvantages, such as discontinuous input current or high voltage rating on capacitors [8], [9]. To overcome these limitations of the classical ZSI, quasi-ZSI (qZSI) was proposed. Although it uses the same number of inductors, capacitors, and diodes, the proposed structure creates a novel connection among these components [10]–[12]. Due to the

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benefits of ZSI and qZSI, they have been validated by many applications, such as photovoltaic (PV) systems and grid connections [13]–[15]. To improve output voltage quality, the ZSI and qZSI are both integrated with a three-level inverter.

In [16], a novel connection between two identical ZS networks was investigated to provide a three-level voltage at the output of an intermediate network. This configuration used two isolated equal sources to feed two ZS networks. The 3LNPCI was installed after the ZS network to provide multilevel inverter characteristics. With the advantages of the connection reported in [16], a new combination involving only one ZS network with the 3LT^{2}I was discussed in [17]. By applying split-DC input source feeding to the ZS network, this configuration provides three-level voltage to an output without requiring more ZS networks [16]. This topology can considerably reduce the required number of passive components without affecting the boost factor of the converter. As a result, size, cost, and control complexity are significantly improved. The 3L-T^{2}I was integrated with the qZS network in [9] and [18] not only to provide satisfactory output voltage quality but also to ensure that the benefits of qZS networks are derived. In this study, two identical qZS networks were connected in a cascade form to enhance the number of output voltage levels by merely utilizing one input source.

Although ZSI and qZSI afford advantages, both topologies also have disadvantages. They require numerous passive components (inductors or capacitors), they have a considerable inductor current ripple, and their boost factor and voltage gain are low. In [19], a qSB (quasi-switched boost) network was introduced to replace the ZS and qZS networks. Two diodes, one inductor, one capacitor, and one active switch comprise the qSB network. This type of intermediate network compared with the ZS and qZS networks reduces the required number of inductors and capacitors by one. The integration of this topology to the 3LNPCI was also proposed to enhance the number of output voltage levels [20]. This study used two identical qSB networks connected in a cascade form to generate three-level output voltage feeding to the 3LNPCI. In the new connection of the qSB network, one inductor was removed and feeding by a single DC source was introduced [21]–[23].

Common-mode voltage (CMV) is one of the critical problems of multilevel inverters. It causes leakage current, shaft voltage, bearing current, and electromagnetic interference [24], [25]. High leakage current through system ground causes system unreliability. The study in [26] has proposed a novel model predictive control for conventional 3L-T^{2}I to reduce the CMV and balance the neutral voltage. Two nearest vectors which have low CMV amplitude are used to produce reference vector. However, it is hard to applied this work to impedance-source network because the ST state is unable to be inserted in some region of space vector diagram. To reduce the CMV amplitude, the work in [27] used zero vector, medium vectors, and large vectors to generate the output voltage. This approach can reduce the CMV magnitude to half of that in the conventional method. The method in [27] was also applied to qZSI in [9] and [28] to enhance the voltage gain of the inverter. In [9], an extra small vector with a low-magnitude CMV was used to balance the neutral voltage without affecting the CMV amplitude. However, the root mean square (RMS) value of CMV is slight increased. In [9] and [28], the buck–boost capability is ensured by a full-ST state added to a zero vector. Nevertheless, the boost factor of these works is low. The work in [22] introduced an SVM method to eliminate the CMV using zero and medium vectors. Compared with [9] and [28], the study in [22] resulted in lower inductor current, higher voltage gain, and lower CMV. However, the output voltage quality of [22] is worse than those reported in [9] and [28]. Furthermore, the modulation index reported in [22] is limited and lower than those reported in [9] and [28]. The work in [23] enhanced the voltage gain, reduced the voltage stress on components, and provided a high output voltage quality compared with those in [9], [22], and [28]. However, the CMV magnitude is considerably larger than those reported in previous studies. In [23], the upper-ST (UST) and lower-ST (LST) states were applied to enhance the voltage gain. The study in [29] achieved the same voltage gain as that in [23] but with a lower CMV amplitude. However, the output voltage quality of the method in [29] was worse than that in [23].

To leverage the advantages of high voltage gain and satisfactory output voltage quality achieved in [23], this paper introduces a new pulse width modulation (PWM) technique based on an SVM to reduce the CMV magnitude. All vectors with high CMV magnitudes are removed from the space vector diagram, and those that produce low CMV are used to generate output voltage. In this scheme, small vectors are still used to insert UST and LST states. As a result, the output voltage quality is maintained compared with that in [23]. The remaining parts of this paper consist of five sections. Section II presents the inverter circuit and some operating states. The SVM method for reducing CMV is proposed in Section III. The overall comparison is discussed in Section IV. The PSIM simulation software and experiment prototype built in the laboratory are used to derive the simulation and experimental results presented in Section V. The summary is presented in Section VI.

II. INVERTER CIRCUIT

Fig. 1 presents the topology of 3L-qSBT^{2}I. In this figure, the conventional three-level T-type inverter is placed after the front-end active impedance-source network to ensure a three-level voltage output. In each leg, three-level voltage is ensured by four switches, S_{jx} ($j = 1, 2, 3, 4; x = a, b, c$). State "$P$" denotes the value $+V_{PN}/2$ at the output pole voltage, V_{xO}, which is generated by activating switches S_{1x} and S_{2x}. State "O" represents the value zero at the output pole voltage, which is ensured by turning on bi-directional switches S_{2x} and S_{3x}. When both switches, S_{3x} and S_{4x}, are simultaneously triggered, the value of $-V_{PN}/2$ is generated at the output. The DC-link voltage, V_{PN}, at the input side of the T-type inverter circuit is generated by the qSB network, which consists of

an inductor (L_B), two capacitors (C_P and C_N), two switches (S_P and S_N), and four diodes (D_1–D_4). The impedance-source network is fed by a single DC source, V_{dc}, as shown in Fig. 1. By applying the front-end qSB circuit between the input voltage and inverter circuit, this topology can achieve ST immunity and buck–boost operation in a single-stage power conversion.

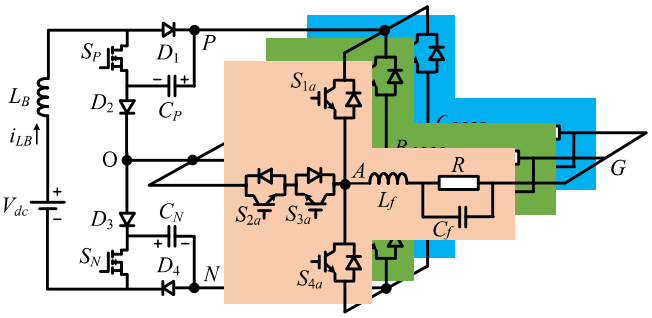

FIGURE 1. Topology of 3L-qSBT^{2}I.

Similar to any single-stage inverters, this topology operates under two main modes: ST and non-ST (NST) modes (Fig. 2). As mentioned in [23], the ST mode consists of UST and LST modes, which are inserted to small vectors to enhance the boost factor and voltage gain of the inverter. In the UST mode, the inverter side can produce two states, "O" and "N," which are ensured by capacitor C_N. Capacitor C_P is disconnected from the main circuit, as shown in Fig. 2(e). Similarly, this C_P capacitor supports the inverter to produce states "P" and "O" under the LST mode, whereas capacitor C_N is disconnected from the power circuit. As shown in Figs. 2, (a)–(d), the NST mode consists of four sub-modes: NST modes 1–4, respectively. In particular, NST mode 3 is generated by triggering switches S_P and S_N of the impedance-source network, which stores energy to the inductor and enhances the boost factor. The on/off state of inverter switches is summarized in Table 1.

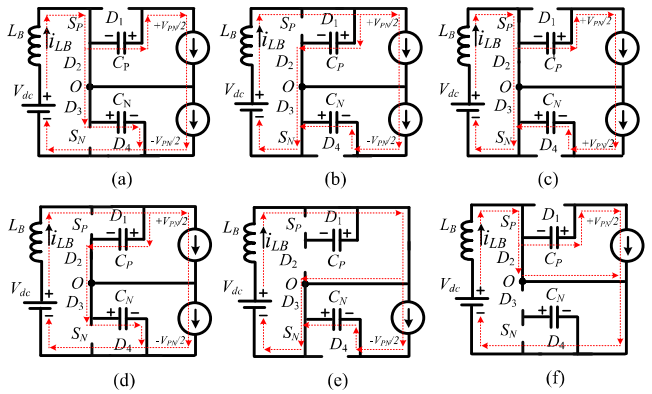

FIGURE 2. Modes of 3L-qSBT^{2}I: (a) NST 1, (b) NST 2, (c) NST 3, (d) NST 4, (e) UST, (f) LST.

III. PROPOSED SVM SCHEME TO REDUCE CMV FOR 3LqSBT^{2}I

The following equation yields the CMV:

$$CMV = V_{GO} = \frac{V_{AO} + V_{BO} + V_{CO}}{3}, \tag{1}$$

TABLE 1. On/Off states of 3L-qSBT^{2}I (x = a, b, c).

Mode	ON Switch	ON Diode	V_{xO}
NST1	S_P	D_2, D_3, D_4	$+V_{PN}/2$, 0, $-V_{PN}/2$
NST2	S_N	D_1, D_2, D_3	$+V_{PN}/2$, 0, $-V_{PN}/2$
NST3	S_P, S_N	D_2, D_3	$+V_{PN}/2$, 0, $-V_{PN}/2$
NST4	S_{1x}, S_{2x}	D_1, D_2, D_3, D_4	$+V_{PN}/2$
	S_{2x}, S_{3x}		0
	S_{3x}, S_{4x}		$-V_{PN}/2$
UST	S_{1x}, S_{2x}, S_{3x}, S_N	D_1, D_3	0 *or* $-V_{PN}/2$
LST	S_{2x}, S_{3x}, S_{4x}, S_P	D_2, D_4	0 *or* $+V_{PN}/2$

where V_{AO}, V_{BO}, and V_{CO} are the output pole voltages of the inverter side.

Based on (1), the CMV amplitude generated by each voltage vector of the inverter can be calculated, as summarized in Table 2. According to the list, the largest CMV values are $\pm V_{PN}/2$, which are achieved by adopting zero vectors, [PPP] and [NNN]. The small vectors have four CMV values: $\pm V_{PN}/6$ and $\pm V_{PN}/3$. The large vectors also generated $\pm V_{PN}/6$. The medium vectors and zero vector, [OOO], have the zero CMV value.

TABLE 2. CMV of 3L-qSBT^{2}I.

Vectors	State	*CMV*	State	*CMV*	State	*CMV*
Zero	[OOO]	0	[PPP]	$+V_{PN}/2$	[NNN]	$-V_{PN}/2$
P-Type Small	[POO]	$+V_{PN}/6$	[PPO]	$+V_{PN}/3$	[OPO]	$+V_{PN}/6$
	[OPP]	$+V_{PN}/3$	[OOP]	$+V_{PN}/6$	[POP]	$V_{PN}/3$
N-Type Small	[ONN]	$-V_{PN}/3$	[OON]	$-V_{PN}/6$	[NON]	$-V_{PN}/3$
	[NOO]	$-V_{PN}/6$	[NNO]	$-V_{PN}/3$	[ONO]	$-V_{PN}/6$
Medium	[PON]	0	[OPN]	0	[NPO]	0
	[NOP]	0	[ONP]	0	[PNO]	0
Large	[PNN]	$-V_{PN}/6$	[PPN]	$+V_{PN}/6$	[NPN]	$-V_{PN}/6$
	[NPP]	$+V_{PN}/6$	[NNP]	$-V_{PN}/6$	[PNP]	$+V_{PN}/6$

In [23], all 12 small vectors are utilized to synthesize the output voltage vector; thus, the CMV is varied from $+V_{PN}/3$ to $-V_{PN}/3$. Although the use of these small vectors enhances the boost factor and voltage gain by improving the ST duty ratio, it also increases the CMV.

In this study, small vectors with low CMV amplitudes ($\pm V_{PN}/6$) are used with the zero vector ([OOO]), medium vectors, and large vectors to reduce the CMV; this differs from that reported in [23]. Note that the use of these vectors does not limit the utilization of the ST duty ratio; thus, the advantage of high voltage gain of [23] is also leveraged in this work.

The space vector diagram of the proposed method is depicted in Fig. 3. In this figure, the space vector diagram is divided into six sectors (sectors I–VI). In each sector, four regions identify the location of the reference vector. Similar to the traditional SVM method, the reference vector is synthesized through three nearest vectors based on its location. The

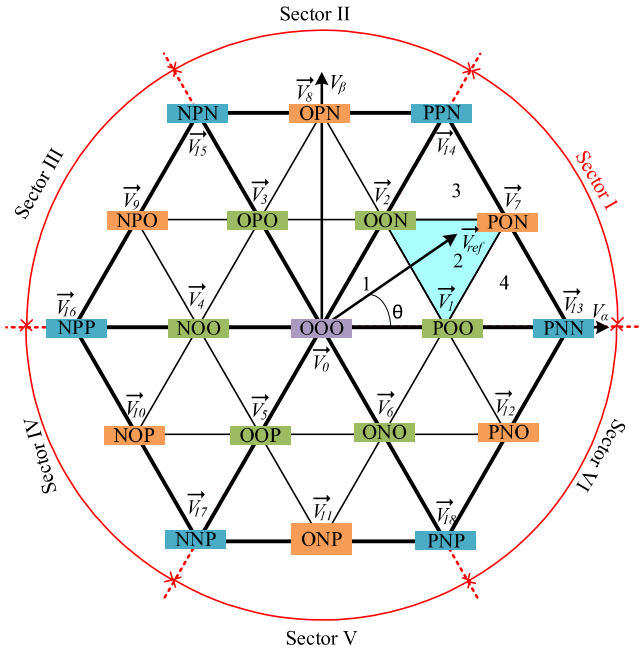

FIGURE 3. Space vector diagram of proposed scheme.

rest of this section presents details regarding vector selection, dwell time calculation, and ST insertion for the proposed SVM method.

A. DWELL-TIME CALCULATION AND SWITCHING SEQUENCE SELECTION

To analyze the proposed technique, the top of the reference vector is assumed to fall in region 2 of sector I, as highlighted in Fig. 3. As a result, three voltage vectors ($\vec{V}_1$, $\vec{V}_2$, and $\vec{V}_7$) are adopted to generate the output voltage vector, $\vec{V}_{ref}$. The following equation has been adopted:

$$\begin{cases} \vec{V}_{ref}.T_s = \vec{V}_1.t_1 + \vec{V}_2.t_2 + \vec{V}_7.t_7 \\ T_s = t_1 + t_2 + t_7, \end{cases} \tag{2}$$

where

$\vec{V}_{ref}$: output voltage vector;
$\vec{V}_7$: medium-voltage vector;
$\vec{V}_1$, $\vec{V}_2$: small-voltage vectors;
T_s: sampling period; and
t_1, t_2, t_7: dwell times of $\vec{V}_1$, $\vec{V}_2$, and $\vec{V}_7$, respectively.

These voltage vectors are expressed by the following set of equations:

$$\begin{cases} \vec{V}_{ref} = MV_{PN}/\sqrt{3}\, e^{j\theta} \\ \vec{V}_1 = V_{PN}/3e^{j0} \\ \vec{V}_2 = V_{PN}/3e^{j\pi/3} \\ \vec{V}_7 = V_{PN}/\sqrt{3}\, e^{j\pi/6}. \end{cases} \tag{3}$$

where M is modulation index.

By substituting (3) to (2), the dwell times of these voltage vectors can be expressed as

$$\begin{cases} t_1 = T_s - 2MT_s \sin(\theta) \\ t_2 = T_s - 2MT_s \sin(\pi/3 - \theta) \\ t_7 = 2MT_s \sin(\theta + \pi/3) - T_s. \end{cases} \tag{4}$$

In conventional CMV reduction method for traditional voltage-source inverter, the switching sequence can be selected as [POO]-[PON]-[OON]. However, the unequal time durations of vectors [POO] and [OON] makes it hardly to insert UST/LST state. If try to use this conventional switching sequence, some disadvantages like worse inductor current profile, high amplitude of low frequency component of inductor current will appear. Thus, under the proposed method, the switching sequence for this region is selected as [PON]-[POO]-[OON]-[PON] and return, as shown in Fig. 4. The UST and LST states are inserted into N-type small [OON] and P-type small [POO] vectors, respectively. In both voltage vectors, phase B is also operated under state "*O*." Thus, the insertion of UST and LST states into phase B is considered to reduce the number of commutations. The details of switching sequence and ST insertion are shown in Fig. 4. To leverage the advantages of the work in [23] in low inductor current ripple and high voltage gain, the switches (S_P and S_N) of the impedance-source network are controlled and simultaneously turned on, as indicated by the yellow highlight in Fig. 4. Compared with the ST signal of the inverter side, this state is delayed by $T_S/4$. Both duty cycles of switches S_P and S_N are enhanced by coefficient D_0 to increase the boost factor.

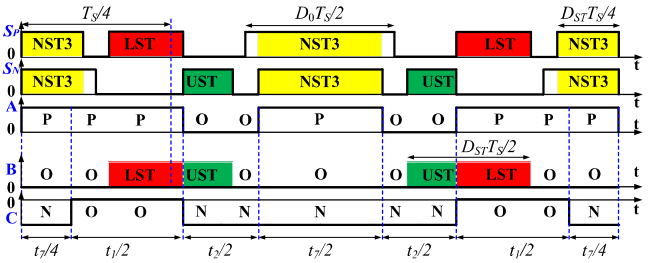

FIGURE 4. Switching sequence in sector I region 2 and control signals of S_P and S_N.

The foregoing can similarly be applied to other regions and sections to calculate the dwell times and select the switching sequence. For example, consider sector I and region 4, shown in Fig. 3, three nearest vectors [POO], [PON], and [PNN] are adopted to synthesize the output voltage vector. In this region, we have only one P-type small vector [POO] and no N-type small vector, thus, the LST insertion is adopted instead of UST insertion. In small vector [POO], phase B and phase C can be utilized to insert LST state. However, in three vectors [POO], [PON], and [PNN], phase B has largest time interval of "O" state, thus, phase B is used to add LST state. The switching sequence is [PNN]-[PON]-[POO]-[PLO]-[POO]-[PON]-[PNN] and return, as shown in Table 3. State "L" denotes the LST state. In this switching sequence, the vector

TABLE 3. Switching sequences of proposed SVM scheme.

Sector	Region	Switching sequence
I	1	[OOO]-[POO]-[PLO]-[OUN]-[OON]-[OOO] and return
	2	[PON]-[POO]-[PLO]-[OUN]-[OON]-[PON] and return
	3	[PPN]-[PON]-[OON]-[OUN]-[OON]-[PON]-[PPN] and return
	4	[PNN]-[PON]-[POO]- [PLO]-[POO]-[PON]-[PNN] and return
II	1	[OOO]-[OPO]-[LPO]-[UON]-[OON]-[OOO] and return
	2	[OPN]-[OPO]- [LPO]-[UON]-[OON]-[OPN] and return
	3	[NPN]-[OPN]-[OPO]-[LPO]-[OPO]-[OPN]-[NPN] and return
	4	[PPN]-[OPN]-[OON]-[UON]-[OON]-[OPN]-[PPN] and return
III	1	[OOO]-[OPO]-[OPL]-[NOU]-[NOO]-[OOO] and return
	2	[NPO]-[OPO]- [OPL]-[NOU]-[NOO]-[NPO] and return
	3	[NPP]-[NPO]-[NOO]-[NOU]-[NOO]-[NPO]-[NPP] and return
	4	[NPN]-[NPO]-[OPO]-[OPL]-[OPO]-[NPO]-[NPN] and return
IV	1	[OOO]-[OOP]-[OLP]-[NUO]-[NOO]-[OOO] and return
	2	[NOP]-[OOP]- [OLP]-[NUO]-[NOO]-[NOP] and return
	3	[NNP]-[NOP]-[OOP]-[OLP]-[OOP]-[NOP]-[NNP] and return
	4	[NPP]-[NOP]-[NOO]-[NUO]-[NOO]-[NOP]-[NPP] and return
V	1	[OOO]-[OOP]-[LOP]-[UNO]-[ONO]-[OOO] and return
	2	[ONP]-[OOP]- [LOP]-[UNO]-[ONO]-[ONP] and return
	3	[PNP]-[ONP]-[ONO]-[UNO]-[ONO]-[ONP]-[PNP] and return
	4	[NNP]-[ONP]-[OOP]-[LOP]-[OOP]-[ONP]-[NNP] and return
VI	1	[OOO]-[POO]-[POL]-[ONU]-[ONO]-[OOO] and return
	2	[PNO]-[POO]- [POL]-[ONU]-[ONO]-[PNO] and return
	3	[PNN]-[PNO]-[POO]-[POL]-[POO]-[PNO]-[PNN] and return
	4	[PNP]-[PNO]-[ONO]-[ONU]-[ONO]-[PNO]-[PNP] and return

U: UST state, L: LST state.

[PLO] is generated by triggering S_{1a}, S_{2a} of phase A leg, S_{2b}, S_{3b}, and S_{4b} of phase B leg, and S_{2c}, S_{3c} of phase C leg. Note that three switches S_{2b}, S_{3b}, and S_{4b} of phase B leg are simultaneously turned on to generate LST state. The output voltage of phase B is still maintained as 0V like conventional vector [POO]. During LST state, the switch S_P of impedance-source network is triggered on to store energy for input inductor. The switching sequences of the proposed method for other regions are summarized in Table 3.

B. STEADY-STATE ANALYSIS

The key waveform of the 3L-qSBT^{2}I under proposed control method is shown in Fig. 5. It can be seen that the inductor voltage is kept at V_{dc} for both UST and LST states. Thus, the boost factor is not affected when the time intervals of UST and LST states are unequal. In steady-state, the average value of inductor voltage is zero. Thus, the capacitor voltages, V_{CP} and V_{CN}, can be calculated using the following equation. Note that $V_{CP} = V_{CN}$, the capacitor voltages are assumed as constant during operation.

$$V_{CP} = V_{CN} = \frac{V_{dc}}{2 - 3D_{ST} - D_0}, \tag{5}$$

where V_{CP}, V_{CN}: capacitor voltages of C_P and C_N;
V_{dc}: DC input source of 3L-qSBT^{2}I;
D_{ST}: ST duty ratio; and
D_0: extra duty ratio of impedance-source network switches (S_P and S_N).

The following equation relates D_{ST} to D_0:

$$D_{ST} \le D_0 \le 1 - D_{ST}. \tag{6}$$

The peak value of the output load voltage can be calculated through the modulation index (M) and DC-link voltage as follows:

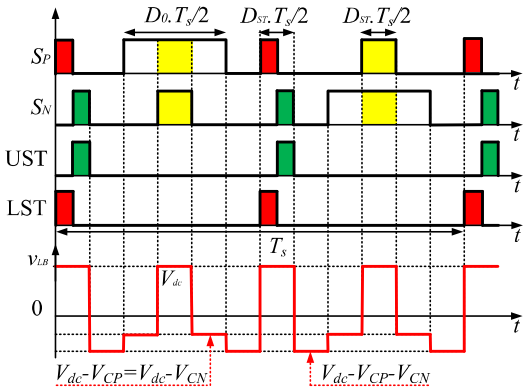

FIGURE 5. Key waveform of impedance-source network control.

$$V_{x,peak} = \frac{2}{\sqrt{3}} \cdot \frac{M.V_{PN}}{2} = \frac{2}{\sqrt{3}} \cdot \frac{MV_{dc}}{2 - 3D_{ST} - D_0}, \tag{7}$$

where $V_{x,peak}$: peak value of output voltage;
M: modulation index; and
V_{PN}: DC-link voltage.

Because the ST state is inserted to small vectors, D_{ST} can be calculated through M using the following equation [23]:

$$\begin{cases} M \le 1 \\ M + D_{ST}/2 \le 1. \end{cases} \tag{8}$$

C. NEUTRAL VOLTAGE BALANCED CONTROL

The neutral voltage imbalanced issue can be addressed by adjusting the extra duty ratio D_0 of switches S_P and S_N of impedance source network. In detail, the time intervals of NST mode 1 and NST mode 2 shown in Figs. 2(a) and 2(b) are used to balance neutral voltage. As shown in Fig. 2(a), when NST mode 1 is adopted, the capacitor C_P is discharged, whereas capacitor C_N is charged. The result is that the C_P voltage is decreased while C_N voltage is increased. In NST mode 2, shown in Fig. 2(b), the C_P voltage is increased while C_N voltage is decreased. In general, the time intervals of these modes are equal which are determined by $(D_0 - D_{ST})T_S/2$. In order to balance neutral voltage, the time intervals of NST mode 1 and 2 are redefined as $(D_1 - D_{ST})T_S/2$ and $(D_2 - D_{ST})T_S/2$, respectively, where D_1 and D_2 are extra duty ratios of switches S_P and S_N. Based on instantaneous voltages of C_P and C_N, two cases are considered to balance neutral voltage: 1) C_P voltage is larger than C_N voltage, and 2) C_P voltage is smaller than C_N voltage. In case 1, the time interval of NST mode 1 should be increased while the time interval of NST mode 2 is decreased. In contrast to case 1, in case 2, the time interval of NST mode 1 should be decreased whereas the time interval of NST mode 2 is increased. Thus, in simply, the duty ratios D_1 and D_2 are obtained as:

$$\begin{cases} D_1 = D_0/2 + k(V_{CP} - V_{CN}) \\ D_2 = D_0/2 - k(V_{CP} - V_{CN}) \end{cases} \tag{9}$$

where k is proportional coefficient.

The coefficient D_1 and D_2 are also satisfied the equation (6).

D. IMPLEMENTATION STEP

The overall implementation of the proposed SVM method is shown in Fig. 6. Firstly, three desired output voltages are transfer to $\alpha\beta$ axis to determine reference vector by using abc/$\alpha\beta$ transformation, as shown in Fig. 6. Based on location of reference vector, three nearest vectors are determined to control output voltages. Note that only vectors, which have low CMV shown in Fig. 2, are selected. Secondly, the dwell-times of candidate vectors are calculated by the same way shown in section III.A. Furthermore, the P-type or N-type small vector of candidate vectors helps to determine whether UST or LST state is selected. Thirdly, the switching sequence has been determined, which shown in Table 3. The capacitor voltage balanced method is obtained by the extra duty ratios D_1 and D_2 of switches S_P and S_N. The detail of this method is shown in section III.C and presented by block diagram in Fig. 6. All these steps are enough to implement the proposed SVM control strategy.

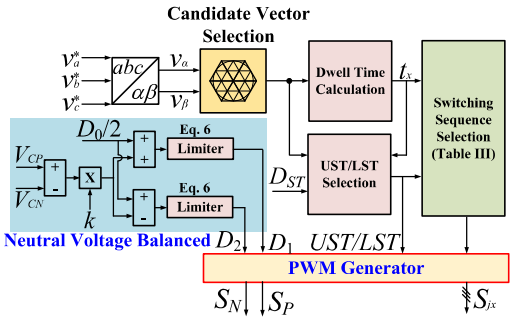

FIGURE 6. Overall implementation of proposed SVM method.

IV. COMPARISON STUDY

The introduced PWM method has been considered for comparison with other single-stage topologies and methods. The overall comparison is summarized in Table 4. Among the works listed in the table 4, the proposed method and SVM method in [23] are superior in using the modulation index, M. With the same value of M, the maximum values of the ST duty ratio (D_{ST}) of the proposed method and the technique presented in [23] are found to be twice those of the other methods. This advantage supports the proposed method in improving the component voltage rating and output voltage quality, as detailed in [23] and [29]. The 3L-qZSI in [9] has the least boost factor and voltage gain leading to the generation of the high DC-link voltage, V_{PN}. For the 3L-qSBT^{2}I topology, the method in [22] results in the smallest voltage gain (Table 4). This limit is explained by the utilization of only zero and medium vectors in the operation. The method in [29] yields the largest boost factor, but the work adopts a small modulation index [29]. Consequently, the same voltage gain is achieved compared with that in [23], as demonstrated in [29].

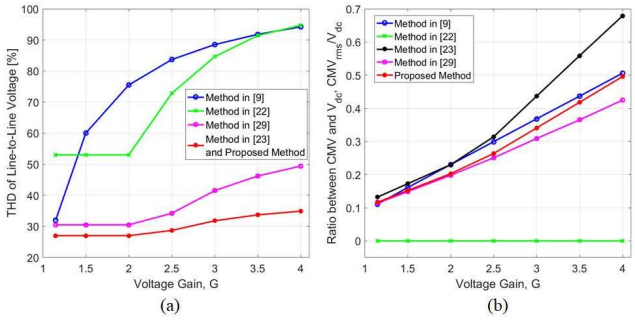

FIGURE 7. Comparison between proposed method and other techniques: (a) voltage gain vs THD of output line-to-line voltage; (b) voltage gain vs. ratio of CMV to input voltage, V_{dc}.

As shown in Fig. 7(a), the THD value of the proposed method and method in [23] is the best. It can be explained that the used of small vectors helps to increase the quality and reduce the THD value of output voltage. In detail, the proposed SVM method with unipolar form of output line-to-line voltage compared with bipolar form of method in [22], produces high output voltage quality than [22], obviously. Moreover, the high voltage gain is applied for this method, it results in high modulation index utilization. This is also one of the reasons to explain for the high quality of output voltage. Although the method in [29] has the same voltage gain and modulation index, the use of zero vector to insert full-ST state results in high THD value of output voltage compared to the proposed method.

As summarized in Table 4, the method in [22] has the lowest CMV magnitude. However, the low voltage gain and the utilization limit of the modulation index are the two main drawbacks of this method. The method presented in [23] yields the largest CMV amplitude (from $-V_{PN}/3$ to $+V_{PN}/3$) because all 12 small vectors are used. The methods in [9] and [29] and the proposed technique can reduce the peak CMV value to half of that in [23] by removing the small vectors, which have large CMV values resulting from the switching sequence. The ratio between the CMV RMS to the input voltage is presented in Fig. 7(b). This figure indicates that the CMV produced by the proposed method is reduced compared with those generated by the methods in [9] and [23]. Although the CMV of the proposed method is larger than those of [22] and [29], the better output quality shown in Fig. 7(a) is among the main advantages of this method.

In summary, the main contribution of this study is the reduction in the CMV magnitude without affecting the voltage gain and modulation utilization compared with [23]. Moreover, the high output voltage quality is one of the important characteristics of this work.

V. SIMULATION AND EXPERIMENTAL RESULTS

A. SIMULATION RESULTS

The proposed SVM method is verified through simulation and experiments; the parameters used are listed in Table 5. The simulation is implemented using PSIM software.

TABLE 4. Overall comparison study.

	3L-qZSI/2-LC [9]	3L-qSBI/1-L [22]	3L-qSBI/1-L [23]	3L-qSBI/1-L [29]	Proposed Method
ST duty ratio, D_{ST}	$1-M$	$1-M$	$2(1-M)$	$1-M$	$2(1-M)$
Boost factor, B*	$1/(1-2D_{ST})$	$2/(1-2D_{ST})$	$2/(1-2D_{ST})$	$2/(1-4D_{ST})$	$2/(1-2D_{ST})$
Output load voltage	$1.15{\cdot}MB/2$	$MB/2$	$1.15{\cdot}MB/2$	$1.15{\cdot}MB/2$	$1.15{\cdot}MB/2$
Voltage gain	Very Low	Low	High	High	High
CMV	$-V_{PN}/6$–$V_{PN}/6$	0	$-V_{PN}/3$–$V_{PN}/3$	$-V_{PN}/6$–$V_{PN}/6$	$-V_{PN}/6$–$V_{PN}/6$
Output line-line voltage pattern	Unipolar	Bipolar	Unipolar	Unipolar	Unipolar
THD of output voltage	88.5% at G = 3	84.6% at G = 3	31.8% at G = 3	41.5% at G = 3	31.8% at G = 3
Output quality	Low	Very Low	Normal	Low	Normal

* Only maximum value is considered

TABLE 5. Simulation and experimental parameters.

Components		Values
DC input source	V_{dc}	100 V ÷ 200 V
Output voltage	$V_{o,RMS}$	110 V_{RMS}
Output frequency	f_o	50 Hz
Switching frequency	f_s	5 kHz
ST duty cycle	D_{ST}	0.16
Extra coefficient	D_0	0.16 ÷ 0.84
Modulation index	M	0.92
Boost inductor	L_B	3 mH/20 A
Capacitors	$C_P = C_N$	2000 µF/400 V
LC filter	L_f and C_f	3 mH and 10 µF
Resistor load	R	40 Ω

The boost inductor value is 3 mH, and the two capacitors of the impedance-source network have a value of 2000 μF. The selected values for the three-phase low-pass filter values to generate approximately 1 kHz of cut-off frequency are 3 mH and 10 μF. The selected theoretical output load voltage is 110 V_{RMS}/50 Hz. The three-phase 40-Ω resistive load is considered to test the proposed scheme in two cases (i.e., two input voltage values): 1) 200-V and 2) 100-V. To achieve 110 V_{RMS} at the output load voltage, the set modulation index, M, and ST duty ratio, D_{ST}, are 0.92 and 0.16, respectively. Under the 200-V input voltage, 0.16 is the selected value for the extra coefficient, D_0; 0.84 is selected for D_0 when adopting the 100-V input voltage. The simulation results are shown in Figs. 8 and 9.

Fig. 8 shows the simulation results for the 200-V input voltage. In this case, the minimum voltage gain is obtained by setting 0.16 as the value for both coefficients, i.e., D_{ST} and D_0. With the above values, the capacitor voltages are boosted to approximately 147-V, as shown in Fig. 8(a). The two capacitor voltage values are balanced. These capacitor voltage values result in the 294-V DC-link voltage, as presented in Fig. 8(a). Note that the DC-link voltage is a pulse wave and varies from 147-V to 294-V because the UST and LST states are used instead of the FST state. The top of the output line-to-line voltage, V_{AB}, is varied from 0 to the peak DC-link voltage value; its Fast Fourier Transform (FFT)

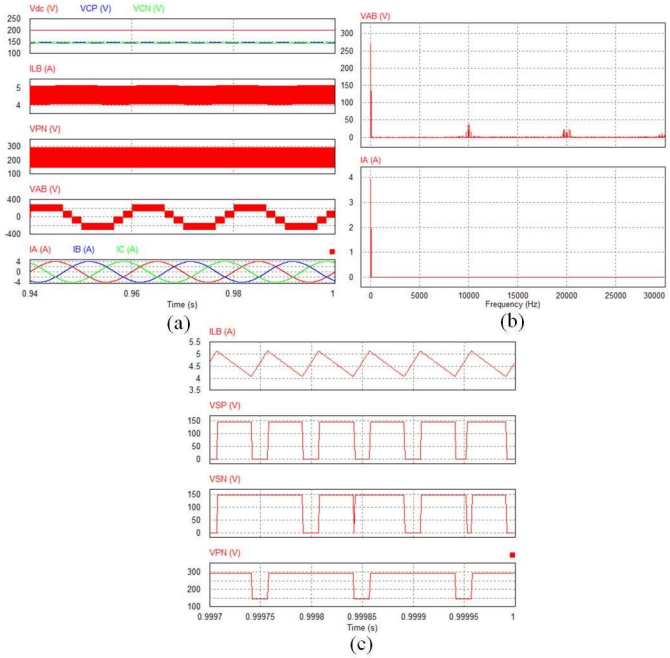

FIGURE 8. Simulation results for proposed method under 200-V input source.

spectrum is shown in Fig. 8(b). The peak value of the first-order harmonic is 269-V. The amplitude of high-frequency harmonic spectrum is mitigated by applying an LC (inductor–capacitor) filter, as shown in the FFT spectrum of the output current in Fig. 8(b). Thus, the output load current is a sinusoidal waveform whose peak value is 3.88-A. The THD values of V_{AB} and I_A are 32.29% and 0.345%, respectively. The average value of the current in inductor L_B is 4.59-A, as shown in Fig. 8(a). Figure 8(c) shows the magnified waveforms of I_{LB}, V_{SP}, V_{SN}, and DC-link voltage V_{PN}. The voltage stresses of switches S_P and S_N are equal to the capacitor voltage. The inductor current frequency (20 kHz) is four times greater than the switching frequency.

Fig. 9 shows the simulation results for the 100-V input voltage. In this case, to achieve 110 V_{RMS} at the output load

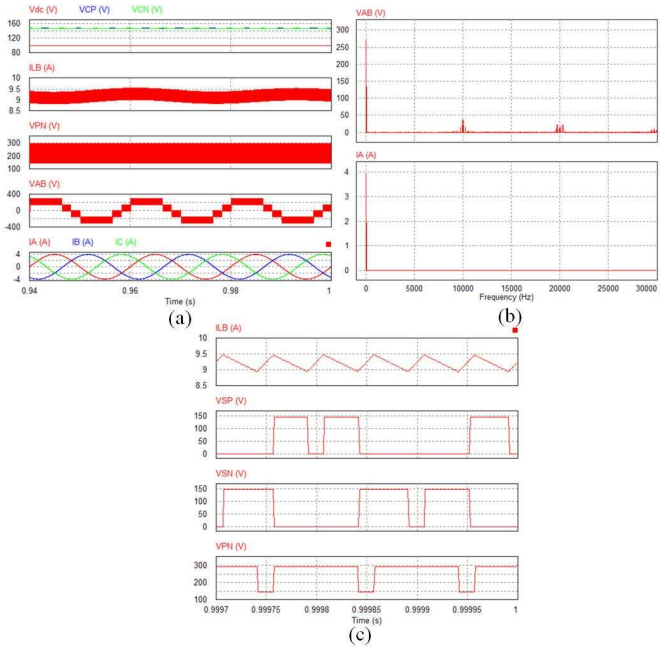

FIGURE 9. Simulation results for proposed method under 100-V input source.

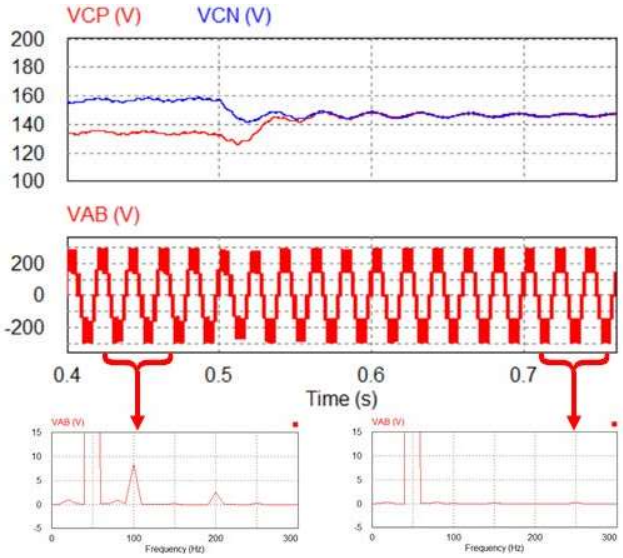

FIGURE 10. Simulation results for neutral voltage balanced control.

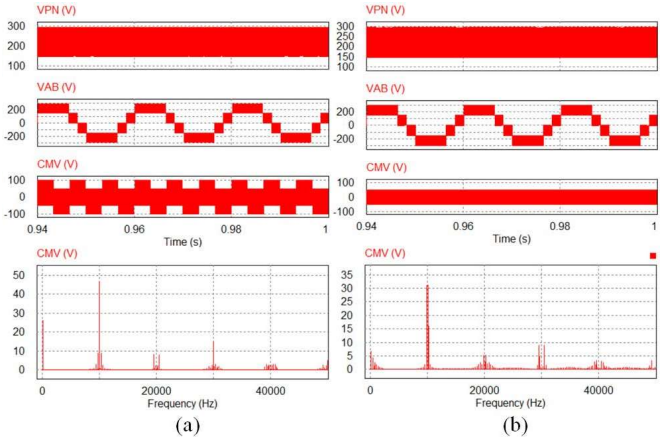

FIGURE 11. Comparison between method in [23] and proposed method: (a) method in [23], (b) proposed method.

voltage, the maximum voltage gain is adopted. The extra coefficient, D_0, is set to 0.84 instead of 0.16. Two capacitor voltage values remain boosted at approximately 147 V from the 100-V input source, as illustrated in Fig. 9(a). The 294-V remains at the DC-link voltage and peak value of the output line-to-line voltage, V_{AB}. From the FFT spectrum of V_{AB} and I_A, the calculated THD values of these waveforms remain as 32.29% and 0.374%, respectively. The average inductor current value is 9.2 A. The frequency of inductor current is also 20 kHz, as shown in Fig. 9(c).

The simulation result of neutral voltage balanced control are shown in Fig. 10. The unbalanced neutral-point voltage causes distortion at output line to line voltage, which results in high amplitude of low frequency components (100Hz and 200Hz) of V_{AB}. After applying the balanced control method, the different between two capacitor voltages is very small, which significantly reduces the magnitude of low frequency components of output line to line voltage.

The CMV comparison between the method in [23] and the proposed method is shown in Fig. 11. It can be seen that the boost characteristics of impedance-source network are the same for both method in [23] and the proposed SVM method, which is shown in DC-link voltage waveform, V_{PN}. The peak-value of V_{PN} is 294V, and V_{PN} waveform is varied from 147 V to 294 V because of adopting UST/LST insertion. The output line-to-line voltages, V_{AB}, have the same THD values which are 32.29% for both methods. Thus, it can conclude that the proposed method maintains the output voltage quality compared to [23]. Moreover, the peak-to-peak value of CMV of proposed method is a half less than that of conventional method in [23]. The RMS values of CMV with the proposed method and strategy in [23] are 35.8 V_{RMS} and 46.4V_{RMS}, respectively. The proposed method reduces 22.8% RMS of CMV compared to the method in [23]. The FFT spectrums of CMV are shown in Fig. 11. It can be seen that, with smaller RMS value of CMV, the proposed method can reduce the amplitude of high-frequency component of CMV compared to the work in [23], significantly. The investigation about CMV of method in [23] and the proposed method with variation of modulation index is shown in Fig. 12. It can be founded that the proposed method always has smaller RMS value of CMV compared to [23]. Both methods have max value of CMV at 0.5 of modulation index because the time interval of small vector is maximized in this case [9], [22], [28].

B. EXPERIMENTAL RESULTS

Experiments for validating the proposed SVM method have been conducted in a laboratory. The parameters are the same as those used in the simulation; both 100-V and 200-V input

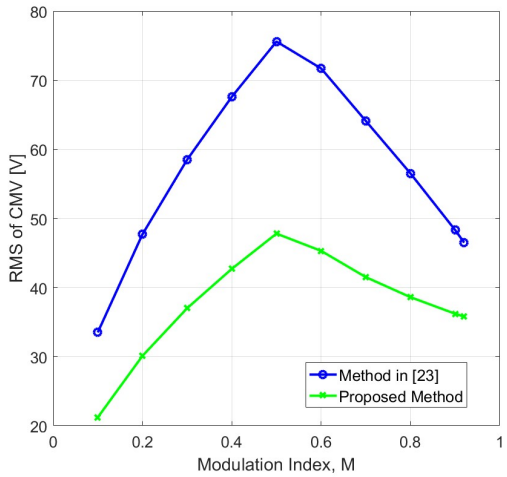

FIGURE 12. CMV comparison between the proposed method and method in [23] in different modulation index values.

voltages are considered to test the inverter. The experimental results are presented in Figs. 13, 14 and 15.

Under the 200-V input source, the two capacitor voltages, V_{CP} and V_{CN}, are boosted to 140 and 141 V, respectively, as shown in Fig. 13(a). The input current is continuous, and its measured average value is 4.78 A. The peak value of DC-link voltage, V_{PN}, is the sum of the two capacitor voltage values, i.e., approximately 280 V, as shown in Fig. 13(b). In this figure, the V_{PN} waveform varies from 140 to 280 V because the proposed method adopts the insertion of the UST and LST states. The output line-to-line voltage, V_{AB}, varies from $-V_{PN}$ to $+V_{PN}$; it has five voltage levels, as illustrated in Fig. 13(b). The output load current is a sinusoidal wave, and its RMS value is 2.59 A_{RMS}. The magnified waveforms of the inductor current, I_{LB}, the voltages values of switches S_P and S_N, and the DC-link voltage are shown in Fig. 13(c). This figure indicates that the operating frequency of the inductor is four times larger than the switching frequency. The high operating frequency reduces the inductor current ripple compared with that yielded by the traditional PWM control method. In Fig. 13(c), the inductor current increases and decreases linearly. It increases in the UST/LST state when the DC-link voltage is half of its peak value. Moreover, when both switches (i.e., S_P and S_N) are activated, the inductor also stores energy.

Under the 100-V DC input source, the extra duty ratio, D_0, increases to 0.84 to maintain the output voltage. In this case, the two capacitor voltages, V_{CP} and V_{CN}, reach 126 and 128 V, respectively. The average inductor current value is 9.35 A, as shown in Fig. 14(a). The DC-link voltage can reach 254 V in the NST mode, as shown in Fig. 14(b). The peak

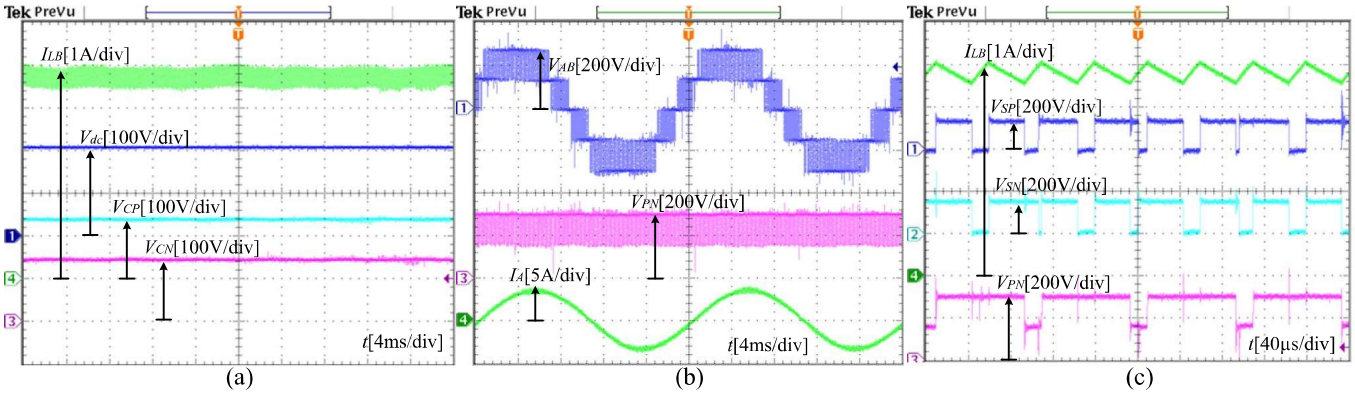

FIGURE 13. Experimental results of proposed method when $V_{dc} = 200$ V. From top to bottom: (a) inductor current, i_{LB}; DC input source, V_{dc}; capacitor voltages, V_{CP} and V_{CN}. (b) Output line-to-line voltage, V_{AB}; DC-link voltage, V_{PN}; output load current, I_A. (c) Inductor current, i_{LB}; switch voltages, V_{SP} and V_{SN}; DC-link voltage, V_{PN}.

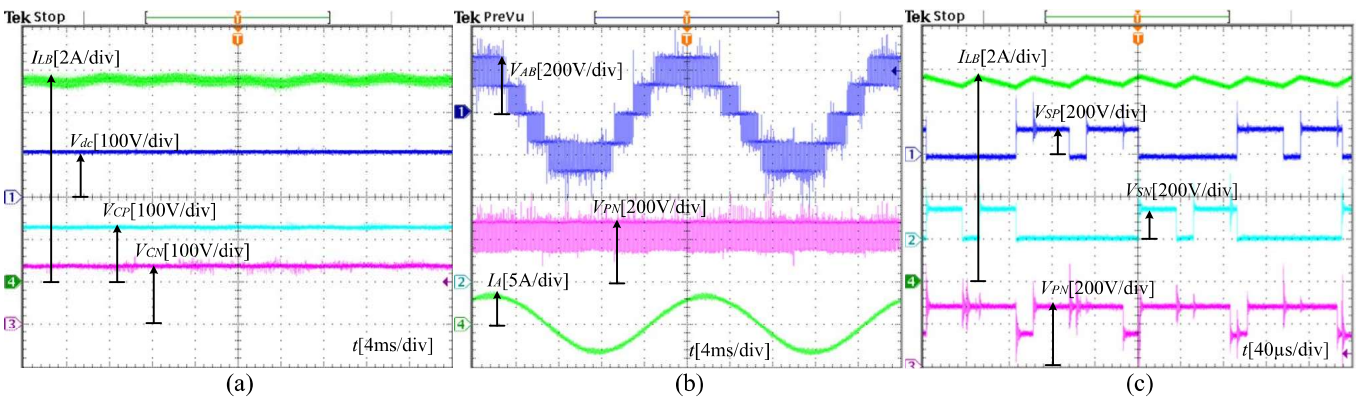

FIGURE 14. Experimental results of proposed method when $V_{dc} = 100$ V. From top to bottom: (a) inductor current, i_{LB}; DC input source, V_{dc}; capacitor voltages, V_{CP} and V_{CN}. (b) Output line-to-line voltage, V_{AB}; DC-link voltage, V_{PN}; output load current, I_A. (c) Inductor current, i_{LB}; switch voltages, V_{SP} and V_{SN}; DC-link voltage, V_{PN}.

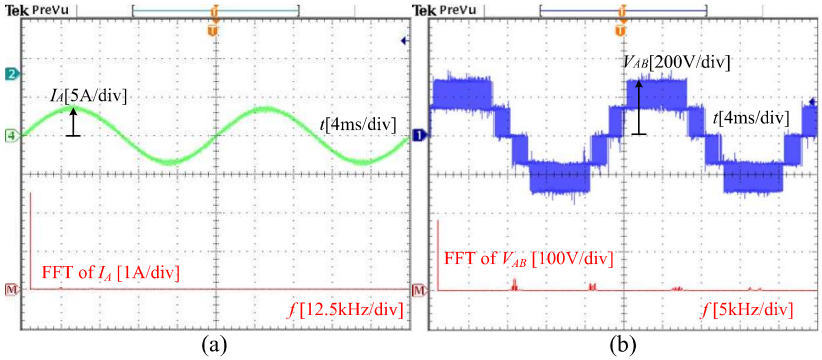

FIGURE 15. FFT spectrum of output load current and output line-to-line voltage.

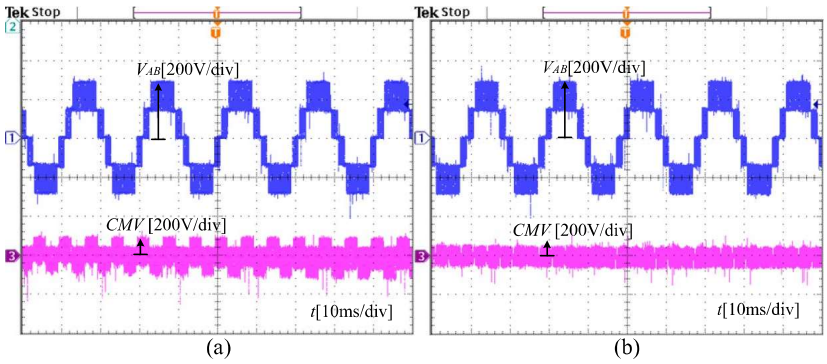

FIGURE 16. Experimental results of conventional and proposed methods: (a) method in [23]; (b) the proposed method.

value of the output line-to-line voltage is also 254 V. The RMS value of the output load current is 2.52 A_{RMS}. With the larger duty ratio, D_0, compared with that in case 1, the on periods of switches S_P and S_N also increase, as shown in Fig. 14(c).

The FFT spectrum of output load current I_A and output line-to-line voltage V_{AB} are presented in Fig. 15. Based on these spectrums the THD value of V_{AB} can be calculated as 45.9%. The high frequency component of output voltage is mitigated by a LC filter, thus, the output load current is sinusoidal waveform, and its THD value is 2.15%.

The proposed method and that in [23] are implemented to prove the effectiveness of the proposed technique to achieve CMV reduction; the results are shown in Fig. 16. In this figure, the proposed method can reduce the peak CMV value by half the CMV value of the conventional method without affecting the output line-to-line voltage. As a result, the quality of the output voltage is maintained. The RMS values of CMV of the proposed and conventional methods are 36.7 and 48.4 V_{RMS}, respectively. This shows that the proposed method can reduce the RMS voltage of CMV by 24.17% compared with the traditional control scheme.

VI. CONCLUSION

A new SVM control method is introduced for the 3L-qSBT^{2}I to reduce the peak-to-peak CMV value. With this approach, the small vectors with small CMV values are used in addition to the zero, medium, and large vectors to generate the output voltage vector. The UST and LST vectors are utilized with traditional vectors to boost the DC-link voltage. Because the UST and LST vectors are added to the small vectors, the inverter achieves high voltage gain. Under the proposed SVM method, some results are obtained: 1) the high voltage gain is achieved with some benefits such as good inductor current profile and low component voltage rating, 2) output voltage quality is improved when compared to previous modulation methods, 3) the peak-to-peak value of CMV is reduced by half of that in conventional SVM method, and 4) the magnitude of high frequency component of CMV is reduced, which reduces the negative impact on the system. The accuracy of the introduced method has been validated by simulation and experiment. The simulation and experimental results show that with the proposed SVM scheme, the peak CMV is reduced to half of that of the conventional method. The RMS value reduction of CMV under the proposed method is around 24.17%.

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Enhanced Boost Factor for Three-Level Quasi-Switched Boost T-Type Inverter

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Abstract: A new modulation strategy has been introduced in this paper in order to enhance the boost factor for the three-level quasi-switched boost T-type inverter (3L-qSBT^{2}I). Under this approach, the component rating of power devices is significantly decreased. Moreover, the use of a larger boost factor produces a smaller shoot-through current. This benefit leads to reducing the conduction loss significantly. Furthermore, the neutral voltage unbalance is also considered. The duty cycle of two active switches of a quasi-switched boost (qSB) network is redetermined based on actual capacitor voltages to recovery balance condition. Noted that the boost factor will not be affected by the proposed capacitor voltage balance strategy. The proposed method is taken into account to be compared with other previous studies. The operation principle and overall control strategy for this configuration are also detailed. The simulation and experiment are implemented with the help of PSIM software and laboratory prototype to demonstrate the accuracy of this strategy.

Keywords: third harmonic injection; single-stage inverter; shoot-through; three-level inverter; quasi-switched boost; T-type inverter

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1. Introduction

Currently, a conventional three-level T-type inverter (3L-T^{2}I) is applied for low voltage applications due to its advantages of low conduction loss due to not using extra diodes compared to neutral point clamped inverter (NPCI) configuration or producing better output quality compared to two-level inverter [1,2]. This topology is recently adopted for many applications, especially photovoltaic (PV) systems and motor drives, etc. [3–5]. Nevertheless, the traditional 3L-T^{2}I produces a low value of AC output voltage in comparison to the input voltage of the inverter. Moreover, the conventional 3L-T^{2}I cannot accept the shoot-through (ST) state during operation because of leading to a short circuit at the DC input source.

Nowadays, impedance-source inverters have been considered as a solution to deal with the drawbacks of conventional inverters [6–8]. By using some passive components such as diodes, capacitors, and inductors in Z-source (ZS) circuit, the ZS inverter (ZSI) can behave as a buck-boost inverter with ST immunity. During operation, the ST state is utilized to belong to traditional vectors of the inverter to enhance the output voltage. The result is that the reliability is significantly improved. According to these advantages, several applications based on ZSI were discussed for the motor drive system, micro-grid connection, and PV applications [9,10]. Many traditional multilevel inverter topologies were considered to incorporate with the ZS network, such as NPCI and 3L-T^{2}I [11–14]. The works in [15,16] introduced a topology combining a single ZS network and 3L-T^{2}I. To ensure a three-level voltage operation, this combination uses a split DC input source. The neutral point of this source is utilized to belong to of ZS circuit to feed to the three-level inverter circuit. This configuration must use one extra diode to guarantee the symmetry of the impedance network. Instead of using full-ST (FST) state, this method used upper-ST (UST) and lower-ST(LST) states to conform to the buck-boost characteristic, which is added

within small vectors. In this strategy, the boost factor is equal to the traditional strategy in [8]. The work in [16] further proposed the neutral voltage balance strategy. However, this strategy required more dwell-time calculations and caused the boost factor effect.

To produce less component voltage rating and draw continuous input current, the quasi-Z-source (qZS) inverter (qZSI) has been presented in [17–22]. These topologies use the same components compared to ZSI, but these components were connected in another way. Like the ZS network, this type of impedance-source structure was considered to incorporate with the three-level inverter to provide multilevel characteristics [17–22]. In these approaches, two qZS circuits are connected to guarantee three-level operation at the output. However, the use of a large number of inductors and capacitors leads to increase volume and decrease power density of the inverter. Furthermore, buck-boost characteristics of the ZS/qZS inverters are only ensured by the ST duty ratio of the inverter branch, which decreases the flexibility of boost factor regulation. The literature [20] introduced the space-vector-modulation (SVM) method and the third harmonic injection scheme, which ensure the buck-boost operation by applying the UST and LST states. Similar to ZSI, these schemes required a split DC source to conduct UST and LST insertions. In [21,22], a novel SVM strategy was proposed to reduce the amplitude and the slew rate dv/dt of common-mode voltage (CMV). In this work, the neutral voltage unbalance problem was handled by adding one more extra small vector into the traditional switching sequence. However, the drew-time of additional small vectors is hardly determined. It produces the complexity of the calculation.

The quasi-switched boost (qSB) inverter (qSBI) was considered as an emerging topology that saves plenty of inductors and capacitors [23–30]. By installing one more active switch in the intermediate circuit, the boost factor of qSBI is so flexible to be controlled [16]. In this configuration, some advantages can be listed as high boost factor and voltage gain and good inductor current profile. These advantages lead to reducing voltage stresses on power devices and less capacitance requirement for passive components such as inductors and capacitors. The works of literature in [25–30] proposed the incorporation between qSB network and the multilevel inverter. In [25,26], the three-level NPCI was combined with two separated qSB networks. The 3L-T^2I was considered to combine with this type of impedance-source network in [27–30]. In [27–30], the qSB network utilized only one inductor and one DC input source, which saves one inductor and a split DC source compared to [25]. These works also proposed a new pulse-width modulation (PWM) strategy based on the phase shift carrier method to provide some benefits such as high voltage gain [21,27], common-mode voltage elimination [28], the capability of operating in normal and open-circuit faults [29], and small component rating. Similar to other types of single-stage buck-boost inverter, this configuration also utilizes the FST state to obtain buck-boost voltage capability, which is inserted within a zero vector to not affect the other voltage vectors. The closed-loop control is employed for capacitor voltage balance, which requires a larger time interval for neutral voltage recovery. The work in [30] adopted a corresponding small vector to balance the neutral voltage. However, this way introduced more CMV amplitude, which is generated by small vectors.

In this paper, a new PWM method is introduced, which improves the boost factor as well as voltage gain of this configuration. The neutral voltage balance is also considered in this paper. Unlike the methods in [16,22,30], where the neutral-voltage balance is ensured by corresponding small vectors of the inverter side, the active switches of the impedance-source network are utilized to balance neutral voltage. The duty cycle difference of these switches is determined based on actual capacitor voltages. This method brings benefits of reducing balancing recovery time and calculation complexity compared to [16,22,27]. The duty cycle of these switches and modulation index are considered to adjust the output voltage of the impedance-source circuit and AC output voltage. The operation modes, as well as the mathematical analysis, will be presented in this paper. Some simulation and experiment setups are used to confirm the accuracy of the proposed modulation method. The rest of this paper consists of four sections as follows. Section 2 introduces the operation

of the inverter and proposed PWM strategy. Section 3 presents a neutral voltage balancing scheme. In Section 4, a comparison study has been conducted to highlight the contribution of this scheme. In Section 5, the simulation and experimental results have been presented to confirm the accuracy of the introduced method. Section 6 presents a conclusion.

2. Proposed PWM Scheme for 3L-qSBT^{2}I

The 3L-qSBT^{2}I is established by an impedance-source network and a 3L-T^{2}I, as observed in Figure 1. The impedance-source network is constructed by two switches S_1 and S_2, four diodes D_1, D_2, D_3, and D_4, two capacitors C_1 and C_2, and one inductor L_B. The outputs of the intermediate circuit are "*P*", "*O*", and "*N*", which are used to ensure the three-level operation of the inverter. The three-phase resistive load is adopted to confirm the operation of the inverter with the proposed scheme, which is fed through a three-phase LC filter to guarantee the sinusoidal waveform of output load voltage with a low THD value, as depicted in Figure 1. The control scheme of this configuration is detailed in the rest of this section. The operating modes, steady-state analysis, and parameter selection are also presented.

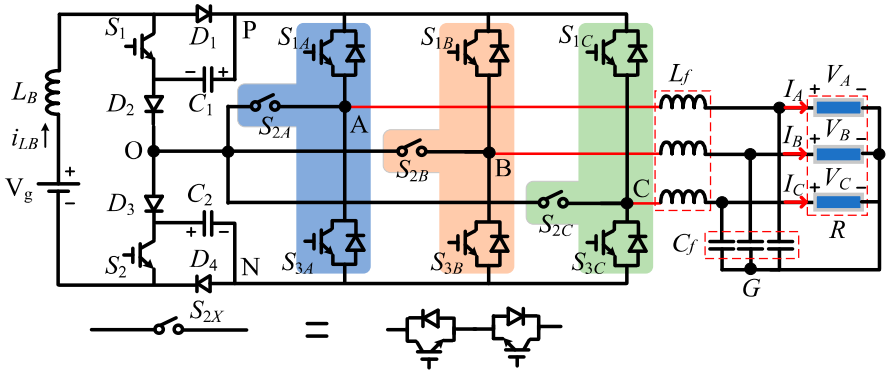

Figure 1. 3L-qSBT^{2}I topology [27].

2.1. PWM Signal Generation

The control method for the 3L-qSBT^{2}I is based on a phase-shift sinusoidal PWM scheme. The PWM control signal generation is divided into two cases: (1) inverter side PWM generation and (2) impedance-source switch PWM generation. For the inverter side, the six reference sinusoidal signals ($\pm v_a$, $\pm v_b$, and $\pm v_c$) are compared with a high-frequency triangle signal (V_{tri1}) to generate control signals for the inverter switches. Figure 2 shows the control signal generation for switches of phase A. In detail, switch S_{1A} is turned on when $-v_a < V_{tri1} < +v_a$, switch S_{3A} is triggered on when $+v_a < V_{tri1} < -v_a$, and switch S_{2A} is turned on when switches S_{1A} and S_{3A} are off. Signals V_{ST} and $-V_{ST}$ are used to create the ST signal denoted by yellow highlight in Figure 2. This ST state is generated by turned on all switches on the inverter side. In order not to affect the output voltage, the V_{ST} must not be smaller than the peak value of reference signals.

For the impedance source side, the triangle signal (V_{tri2}) is used, which is shifted 90 degrees compared to V_{tri1} to create the control signals for the active switches of the impedance-source network [27]. Signals V_{ST} and $-V_{ST}$ are also used with V_{tri2} to generate the ST signal of the intermediate network, which is denoted by green highlight, as shown in Figure 2. Furthermore, two control signals, V_{con1} and V_{con2}, are further used to enhance the duty ratio of S_1 and S_2, as illustrated in Figure 2.

2.2. Operating Modes

Based on the PWM strategy presented in Figure 2, the inverter can be operated under two modes which are ST and non-ST (NST) modes. These modes are divided into five modes, which are ST mode, NST mode 1, NST mode 2, NST mode 3, and NST mode 4,

as observed in Figure 3. To simplify, in non-ST modes, the inverter side is considered a current source, i_O. The on switches and forwarded diodes are shown in Table 1.

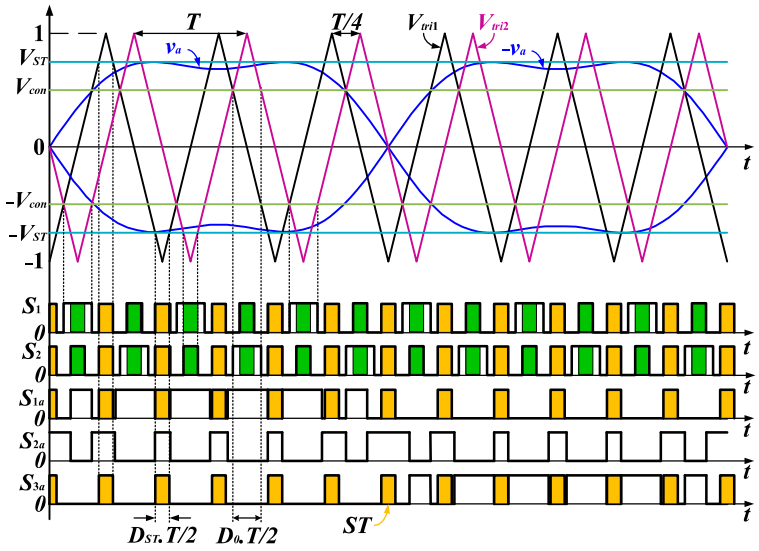

Figure 2. The proposed PWM scheme.

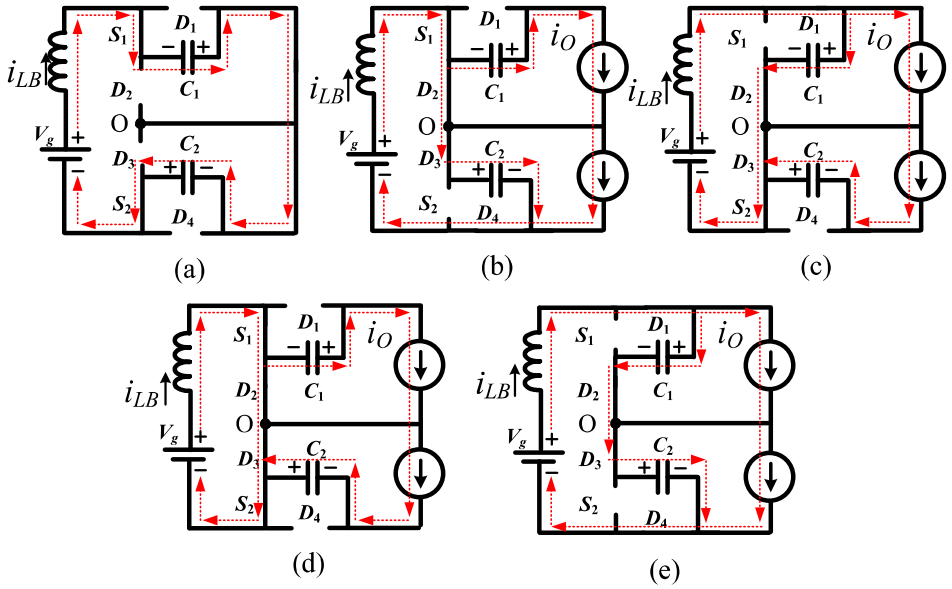

Figure 3. The modes of 3L-qSBT^{2}I: (**a**) ST mode, (**b**) NST mode 1, (**c**) NST mode 2, (**d**) NST mode 3, and (**e**) NST mode 4.

Table 1. On/Off states of 3L-qSBT^{2}I switches and diodes (X = A, B, C).

Mode	ON Switches	ON Diodes	V_{XO}
NST mode 1	S_1	D_2, D_3, D_4	$+V_{PN}/2$, 0 or $-V_{PN}/2$
NST mode 2	S_2	D_1, D_2, D_3	$+V_{PN}/2$, 0 or $-V_{PN}/2$
NST mode 3	S_1, S_2	D_2, D_3	$+V_{PN}/2$, 0 or $-V_{PN}/2$
NST mode 4	S_{1X} S_{2X} S_{3X}	D_1, D_2, D_3, D_4	$+V_{PN}/2$ 0 $-V_{PN}/2$
ST mode	S_1, S_2, S_{1X}, S_{2X}, S_{3X}		0

In ST mode, both switches S_1 and S_2 of the qSB circuit and all switches of inverter side are turned on at the same time. The result is that input inductor L_B is stored energy from the input source and C_1 and C_2 capacitors, as shown in Figure 3a. Conversely, methods in [27,30] only turned on all switches of inverter side, which decrease energy stored in the inductor and boost factor. The voltage across inductor L_B and current across two capacitors are expressed as

$$\begin{cases} L_B \frac{di_{LB}}{dt} = V_g + V_{C1} + V_{C2} \\ C_1 \frac{dv_{C1}}{dt} = C_2 \frac{dv_{C2}}{dt} = -i_{LB} \end{cases} \quad (1)$$

In NST mode 1 and NST mode 2, as shown in Figure 3b,c, capacitors C_1 and C_2 are respectively charged from the DC input source and the energy of inductor L_B. The following equations are obtained as

$$\begin{cases} L_B \frac{di_{LB}}{dt} = V_g - V_{C2} \\ C_1 \frac{dv_{C1}}{dt} = -i_O,\ C_2 \frac{dv_{C2}}{dt} = i_{LB} - i_O \end{cases} \quad (2)$$

$$\begin{cases} L_B \frac{di_{LB}}{dt} = V_g - V_{C1} \\ C_1 \frac{dv_{C1}}{dt} = i_{LB} - i_O,\ C_2 \frac{dv_{C2}}{dt} = -i_O \end{cases} \quad (3)$$

where i_O is the equivalent output current.

In NST mode 3, as illustrated in Figure 3d, the inductor L_B is stored energy from the DC input power supply, whereas two capacitors, C_1 and C_2, transfer energy to the load. The inductor voltage and capacitor currents are expressed as

$$\begin{cases} L_B \frac{di_{LB}}{dt} = V_g \\ C_1 \frac{dv_{C1}}{dt} = C_2 \frac{dv_{C2}}{dt} = -i_O \end{cases} \quad (4)$$

NST mode 4 is shown in Figure 3e, the lower capacitor and upper capacitor are further stored energy in NST modes 1 and 2. In these modes, the voltage across the input inductor and capacitor currents are calculated as

$$\begin{cases} L_B \frac{di_{LB}}{dt} = V_g - V_{C1} - V_{C2} \\ C_1 \frac{dv_{C1}}{dt} = C_2 \frac{dv_{C2}}{dt} = i_{LB} - i_O \end{cases} \quad (5)$$

2.3. Steady-State Analysis

The key waveform of inductor current i_{LB} and capacitor voltages V_{C1} and V_{C2} are depicted in Figure 4. Considering one switching period, the time intervals of ST state is $D_{ST}.T$. The time interval of NST mode 3 is also $D_{ST}.T$. The total time interval of NST mode 1 and NST mode 2 is $(D_0 - D_{ST})$T. The rest time of switching period is $(1 - D_0 - D_{ST})T$, which is the time interval of NST mode 4. The average values of inductor voltage ($\overline{V}_{LB}$) and capacitor currents ($\overline{I}_{C1}$, $\overline{I}_{C2}$) are calculated as in Equation (6). Noted that the following equations are achieved by considering $V_{C1} = V_{C2}$.

$$\begin{cases} \overline{V}_L = [(V_g + 2V_{C1})D_{ST}T + (V_g - V_{C1})(D_0 - D_{ST})T \\ +V_g D_{ST}T + (V_g - 2V_{C1})(1 - D_0 - D_{ST})T]/T \\ \overline{I}_{C1} = \overline{I}_{C2} = [-i_{LB}D_{ST}T - i_O(D_0 - D_{ST})T/2 + (i_{LB} - i_O)(D_0 - D_{ST})T/2 \\ -i_O D_{ST}T + (i_{LB} - i_O)(1 - D_0 - D_{ST})T]/T \end{cases} \quad (6)$$

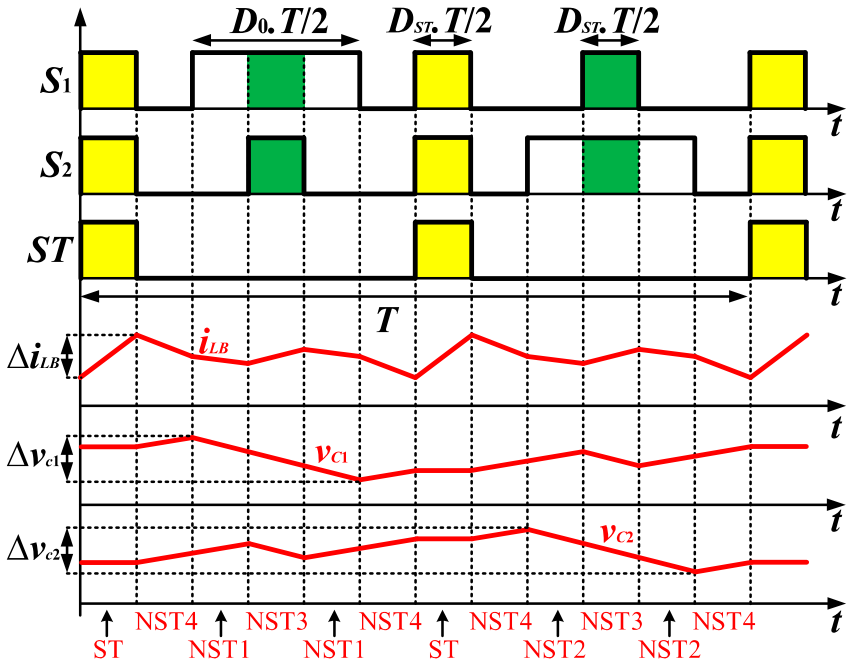

Figure 4. The key waveform in switching period.

In steady-state, these average values are equal to zero, thus the capacitor voltages and average value of inductor current can be expressed as:

$$\begin{cases} V_{C1} = V_{C2} = \frac{V_g}{2-5D_{ST}-D_0} \\ I_{LB} = 2i_O\frac{1-D_{ST}}{2-5D_{ST}-D_0} \end{cases} \quad (7)$$

The max value of V_{PN} voltage is identified by summing of two capacitor voltages and expressed as

$$V_{PN} = V_{C1} + V_{C2} = \frac{2V_g}{2-5D_{ST}-D_0} \quad (8)$$

The boost factor is defined as

$$B = \frac{V_{PN}}{V_g} = \frac{2}{2-5D_{ST}-D_0} \quad (9)$$

The first-order of output load voltage is identified as

$$V_{x,peak} = 1.15MV_{PN}/2 = \frac{1.15MV_g}{2-5D_{ST}-D_0} \quad (10)$$

The voltage gain, G, is calculated as

$$G = \frac{V_{x,peak}}{V_g/2} = \frac{2{\cdot}1.15M}{2-5D_{ST}-D_0} \quad (11)$$

The relationship between two coefficients, D_{ST} and D_0, is defined as

$$D_{ST} \le D_0 \le 1 - D_{ST} \quad (12)$$

From Equation (12), by adopting D_{ST} and $1 - D_{ST}$ for the coefficient D_0, the minimum and maximum voltage gain is identified by the following equation, noting that the value $(1 - M)$ is employed for D_{ST}

$$\begin{cases} G_{\min} = 1.15M/(3M-2) \\ G_{\max} = 2{\cdot}1.15M/(6M-5) \end{cases} \tag{13}$$

2.4. Parameter Selection

The inductor current ripple (Δi_{LB}), illustrated in Figure 4, is calculated with the help of Equation (1) as

$$\Delta i_{LB} = \frac{1}{2L_B f_s} V_g D_{ST} \left(1 + \frac{2}{2 - 5D_{ST} - D_0}\right) \tag{14}$$

where f_s is the switching frequency.

Inductance, L_B, is selected in term of $\Delta i_{LB}/i_{LB} \leq \%x$ as

$$L_B \geq \frac{\mu}{2P_O \%x f_s} V_g^2 D_{ST} \left(1 + \frac{2}{2 - 5D_{ST} - D_0}\right) \tag{15}$$

where $\%x$, μ, and P_O are the maximum percentage of inductor current ripple, the inverter efficiency, and the output power.

The peak-to-peak value of capacitor voltages, V_{C1} and V_{C2}, illustrated in Figure 4, is calculated as

$$\Delta v_{C1} = \Delta v_{C2} = \frac{1}{2Cf_s} D_0 i_O \tag{16}$$

The selection of capacitors, C_1 and C_2, is conducted in terms of $\Delta v_C/V_C \leq \%y$ as follows

$$C_1 = C_2 \geq \frac{1}{4\%y f_s} D_0 \frac{P_O (2 - 5D_{ST} - D_0)^2}{\mu V_g^2 (1 - D_{ST})} \tag{17}$$

where $\%y$ is the maximum percentage of capacitor voltage ripple.

The voltage stresses of impedance switches and diodes are the same as capacitor voltage. The max currents of switches and diodes of the qSB circuit are equal to the max value of the current across the inductor ($i_{LB,peak}$), which is calculated as

$$i_{LB,peak} = \frac{\mu P_O}{V_g} + \frac{1}{4L_B f_s} V_g D_{ST} \left(1 + \frac{2}{2 - 5D_{ST} - D_0}\right) \tag{18}$$

The current stresses of 3L-T^{2}I switches are selected as

$$\begin{cases} I_{Sxy} = i_O, & \text{when} \quad 13D_{ST} + 3D_0 \leq 4 \\ I_{Sxy} = i_{LB}/3, & \text{when} \quad 13D_{ST} + 3D_0 > 4 \end{cases} \tag{19}$$

where S_{xy} (x = 1, 2, 3; y = A, B, C) is the inverter side switch. The voltage across S_{1X} and S_{3X} is the same as the DC-link voltage, whereas it is half of the capacitor voltage for bidirectional switches.

3. Proposed Capacitor Voltage Balance Scheme and DC-Link Voltage Control

As illustrated in Figure 3b, in NST mode 1, the capacitor C_1 is discharged, whereas the capacitor C_2 is stored energy from the input DC source and the input inductor L_B. Therefore, in this mode, the voltage across C_1 is reduced, while C_2 voltage is raised. As opposed to NST mode 1, the C_1 voltage is raised, while the C_2 voltage is reduced, in NST mode 2, as illustrated in Figure 3c. Noted that these modes generate the same inductor voltage, $V_{LB} = V_g - V_C$, in terms of achieving a small difference between two capacitor voltages. Therefore, the boost factor is not much affected when replacing the NST mode 1 to NST mode 2, and vice versa.

To achieve a balancing condition, the proposed method replaces the NST mode 2 with NST mode 1 when $V_{C1} > V_{C2}$. Conversely, NST mode 2 is utilized instead of NST mode 1 when $V_{C2} > V_{C1}$, as presented in Figure 5. The S_1 and S_2 pulses are responsible for doing this work, which is detailed as follows. First, the traditional pulses of S_1 and S_2 are generated by using the V_{tri2}, $\pm V_{ST}$, and $\pm V_{con}$, as shown in Figure 5. Then, V_{C1} and V_{C2} are considered to generate the final pulses of S_1 and S_2. Accordingly, the duty ratio of S_2 is enhanced when $V_{C1} > V_{C2}$. In contrast, the pulse of switch S_1 is enhanced when $V_{C2} > V_{C1}$.

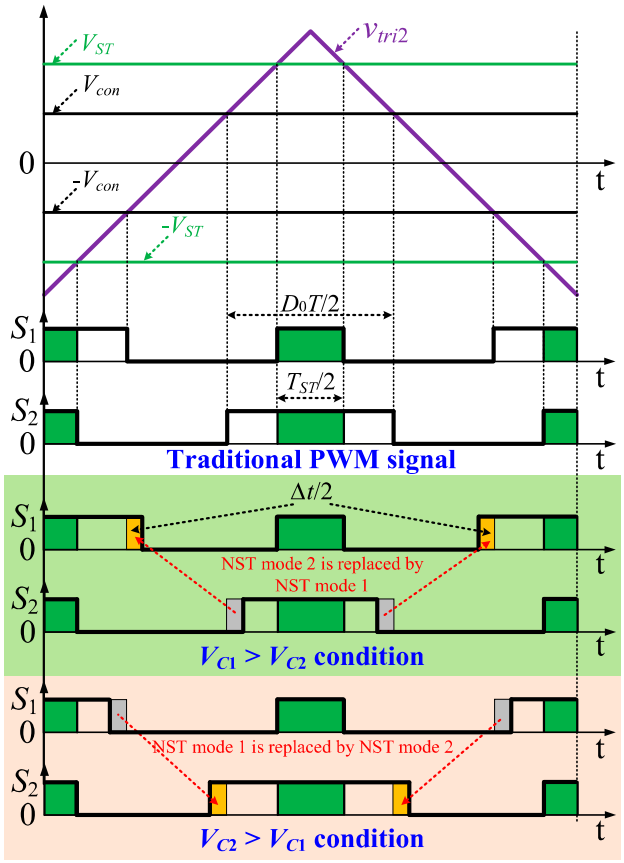

Figure 5. PWM generation for capacitor voltage balance.

In order to detail this strategy, the difference between the two capacitor voltages is defined as

$$v_{dif} = V_{C1} - V_{C2} \tag{20}$$

where:

v_{dif}—the difference voltage between V_{C1} and V_{C2}.

The total time offset, which is used to replace the NST mode 1 with NST mode 2 and vice versa, is identified as

$$\Delta t = \alpha t_{NST1} = \alpha t_{NST2} = \alpha(D_0 - D_{ST})T/2 \tag{21}$$

where:

Δt—the time offset between NST mode 1 and NST mode 2 in one switching period;

t_{NST1} and t_{NST2}—the traditional time intervals of the NST mode 1 and NST mode 2, respectively:

α—is the offset duty ratio ($0 < \alpha \leq 1$).

The capacitor voltage balance strategy is analyzed in two cases that depend on the sign of v_{dif}.

In case 1, the sign of v_{dif} is positive. To achieve capacitor voltage balance, in each switching period, the total time of the $NST1$ and $NST2$ can be redefined as

$$\begin{cases} t'_{NST1} = t_{NST1} + \Delta t = (1+\alpha)(D_0 - D_{ST})T/2 \\ t'_{NST2} = t_{NST2} - \Delta t = (1-\alpha)(D_0 - D_{ST})T/2 \end{cases} \quad (22)$$

where t'_{NST1} and t'_{NST2} are the redefined time interval of NST mode 1 and NST mode 2 in one switching period.

In case 2, the sign of v_{dif} is negative. To obtain capacitor voltage balance, in each switching period, the total time of NST mode 1 and NST mode 2 can be redefined as

$$\begin{cases} t'_{NST1} = t_{NST1} - \Delta t = (1-\alpha)(D_0 - D_{ST})T/2 \\ t'_{NST2} = t_{NST2} + \Delta t = (1+\alpha)(D_0 - D_{ST})T/2 \end{cases} \quad (23)$$

Noted that the larger value of α leads to the faster neutral voltage balance speed. Moreover, having a fixed difference time Δt between on-times of switches S_1 and S_2 makes this scheme easier to be employed than the method in [27]. As mentioned above, in this method, the operation of the inverter side is maintained, and the replacement of NST modes 1 and 2 produces the same voltage across the boost inductor. Therefore, this work does not affect the boost factor and voltage gain.

The control block diagram for the inverter is presented in Figure 6. In this figure, the controller consists of two separated parts, the DC-link voltage and AC output voltage regulations. From Equation (8), V_{PN} can be regulated through two coefficients, D_{ST} and D_0. Like [27], this scheme also fixes the value D_{ST} based on the DC source range. The result is that V_{PN} is controlled through coefficient D_0. Based on Equation (10), the AC output voltage control is achieved by adjusting capacitor voltage and modulation index M. However, when V_{PN} regulation is obtained, the capacitor voltage is fixed at half of DC-link voltage $V_{PN}/2$. Therefore, the AC voltage regulation is obtained by selecting the corresponding value of M.

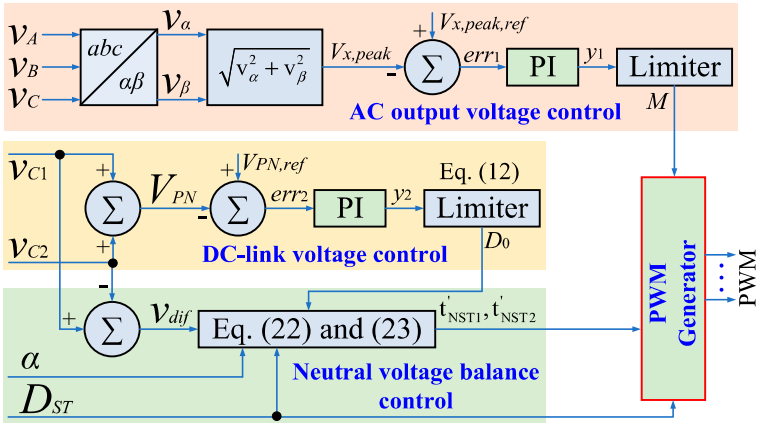

Figure 6. Coordinate control between capacitor voltage balance and DC-link voltage regulation.

For the DC-link voltage regulation, the actual value of V_{PN} is obtained by totaling V_{C1} and V_{C2}. The difference between V_{PN} and the desired DC-link voltage, $V_{PN,ref}$, is minimized by applying the PI controller. The coefficient D_0 is reached by limiting the output of the PI controller by (12).

For the AC output voltage regulation, the actual output voltages (v_A, v_B, v_C) are utilized to calculate the actual $V_{x,peak}$. The abc/αβ transformation is used to obtain this work, as shown in Figure 6. In this scenario, the PI controller is also considered to generate the modulation index M, noted that modulation index M is limited as $(1 - D_{ST})$.

After calculating three coefficients M, D_{ST}, and D_0, the proposed scheme can generate the control signals of inverter switches similar to the conventional scheme. Noted that the

time intervals of NST mode 1 and NST mode 2 have been adjusted, as mentioned above, to obtain neutral voltage balance.

4. Comparative Study

In Section 4, the superior of the proposed method is demonstrated by comparing it to other single-stage inverters and schemes. The PWM strategies of 3L-qSBI in [27,30] are considered to make the comparison with the proposed method. The overview of boost factor, voltage gain, etc., comparison can be observed in Table 2 and Figure 7. In literature [27,30], the comparison between the qSBI, ZSI, and qZSI has been already conducted. It proved that the PWM method in [27,30] provides the highest boost factor and lowest component rating over other single-stage inverters. To simplify, only the PWM method in [27,30] is considered in comparison to the proposed method. It should be noted that the method in [27] is implemented with a third harmonic injection scheme instead of the sinusoidal scheme. This change increases the voltage gain of the method [27] to 1.15 times and does not affect the operation of the inverter. To achieve the highest performance, the D_{ST} is set to $(1 - M)$ for the proposed method and the method in [27]. For the method in [30], the D_{ST} is set to $2(1 - M)$. In these methods, both the maximum boost and minimum boost schemes are investigated. The max boost control is achieved by setting D_0 to $(1 - D_{ST})$, and the min boost control is obtained by applying D_{ST} to D_0.

Table 2. Overall comparison study of the proposed method and strategies in [27,30] for 3L-qSBT^{2}I.

	Strategy in [27]	**Strategy in [30]**	**Proposed Method**
Max ST duty ratio, D_{ST}	$1 - M$	$2(1 - M)$	$1 - M$
Boost factor, B	$2/(3 - 2D_{ST} - D_0)$	$2/(3 - 2D_{ST} - D_0)$	$2/(3 - 5D_{ST} - D_0)$
Voltage gain, G	$1.15{\cdot}MB$	$1.15{\cdot}MB$	$1.15{\cdot}MB$
Capacitor voltage rating, V_c/V_{dc}	$1/(3 - 2D_{ST} - D_0)$	$1/(3 - 2D_{ST} - D_0)$	$1/(3 - 5D_{ST} - D_0)$
Diode voltage rating, V_D/V_{dc}	$1/(3 - 2D_{ST} - D_0)$	$1/(3 - 2D_{ST} - D_0)$	$1/(3 - 5D_{ST} - D_0)$
Switch voltage rating, V_S/V_{dc}	$1/(3 - 2D_{ST} - D_0)$	$1/(3 - 2D_{ST} - D_0)$	$1/(3 - 5D_{ST} - D_0)$

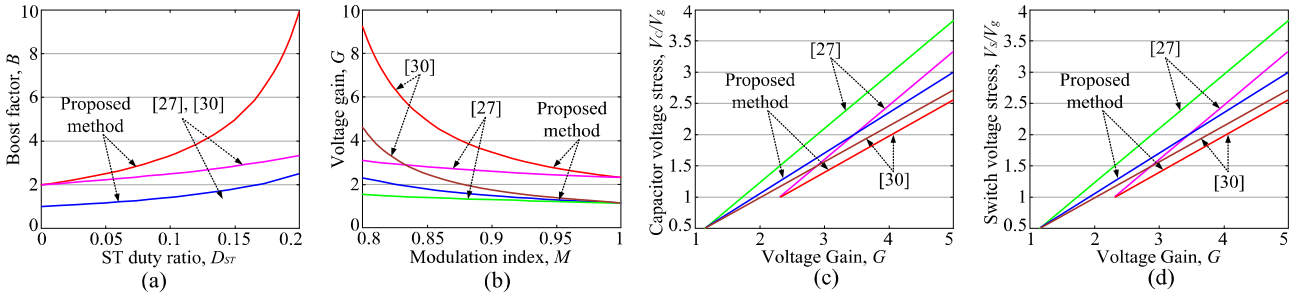

Figure 7. (**a**) The ST duty ratio vs boost factor, (**b**) modulation index vs voltage gain, (**c**) voltage gain vs capacitor voltage rating, and (**d**) voltage gain vs switch voltage rating.

As shown in Figure 7a, when applying the same ST duty ratio, the boost factors, B, of the methods in [27,30] are the same, whereas the proposed method provides the largest boost factor. In voltage gain comparison, the proposed method and the method in [30] are the same, which is larger than that of the method in [27], for the same modulation index, M, as observed in Figure 7b. Due to having a larger boost factor, the proposed method needs a smaller D_{ST} than that of the methods in [27,30] for the same voltage gain. For example, when applying max boost control, if the proposed method needs the value k for D_{ST} to produce voltage G, the value of D_{ST} for the methods in [27,30] must be $(1 + 2k)/(3k)$ and $2k$, respectively. Noted that the most conduction loss of the single-stage inverter is mostly produced in ST mode, thus having smaller D_{ST} makes the proposed method produce less conduction loss than [27,30].

The capacitor voltage rating comparison is illustrated in Figure 7c. It proves that the proposed scheme has smaller voltage stress on the capacitor compared to the method

in [27]. As mentioned in Section 4, the voltage stress on impedance-source switches and diodes are the same as capacitor voltage, while voltage stresses of upper and lower switches of inverter side S_{1X}, S_{3X} ($X = A, B, C$) are twice the capacitor voltage and that is half of the capacitor voltage for bidirectional switches. Therefore, the reduction of capacitor voltage stress causes a reduction of component rating of switches, as presented in Figure 7d.

In summary, the proposed method has produced the largest boost factor and voltage gain over other single-stage three-level buck-boost inverters such as ZSI and qSBIs. These advantages can cause capacitor voltage rating and semiconductor voltage rating reduction. Moreover, the largest boost factor can lead to reducing the conduction loss, which increases the overall efficiency of the inverter.

5. Simulation and Experimental Verifications

5.1. Simulation Results

With the help of PSIM simulation software, the simulation is conducted to validate the operation of the inverter under the proposed method. The simulation parameters are listed in Table 3. Both maximum and minimum boost factor control methods are validated with DC input range from 70 V to 200 V. In both cases, M and D_{ST} are set as 0.76 and 0.15, respectively. The extra duty ratio, D_0, of switches S_1 and S_2 is set to 0.15 and 0.85 to achieve the min and max boost factors, respectively. With these control parameters, the AC output load voltage is maintained at 110 V_{RMS}. The simulation results for both cases are shown in Figures 8 and 9.

Table 3. Simulation and experiment parameters.

Parameter/Components		Values
Input voltage	V_g	70 V ÷ 200 V
Output load voltage	$V_{x,RMS}$	110 V_{RMS}
Output frequency	f_o	50 Hz
Switching frequency	f_s	10 kHz
Extra duty ratio	D_0	0.15 ÷ 0.85
ST duty ratio	D_{ST}	0.15
Modulation index	M	0.76
Boost inductors	L_B	3 mH/20 A
Capacitors	$C_1 = C_2$	2200 µF/400 V
LC filter	L_f and C_f	3 mH and 10 µF
Resistor load	R	56 Ω

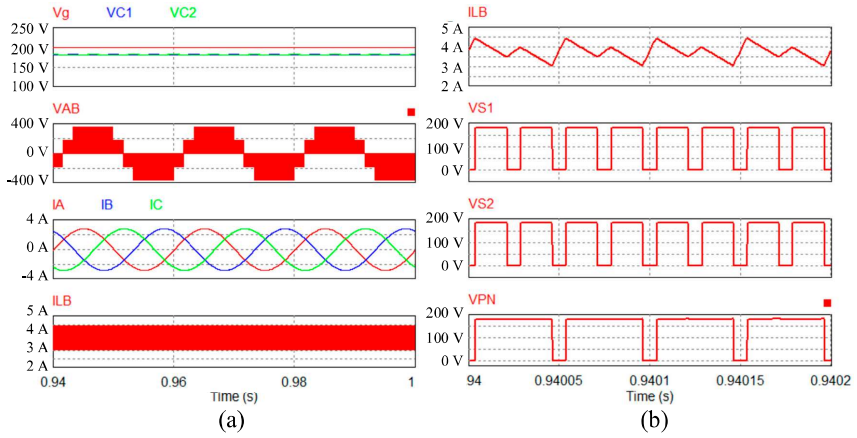

Figure 8. The simulation results of the proposed method when V_g = 200 V. From top to bottom: (**a**) input voltage (V_g), capacitor voltage (V_{C1}, V_{C2}), line-to-line voltage (V_{AB}), load current (I_A, I_B, I_C), inductor current (I_{LB}), (**b**) zoom in of inductor current (I_{LB}), impedance switch voltages (V_{S1}, V_{S2}), DC-link voltage (V_{PN}).

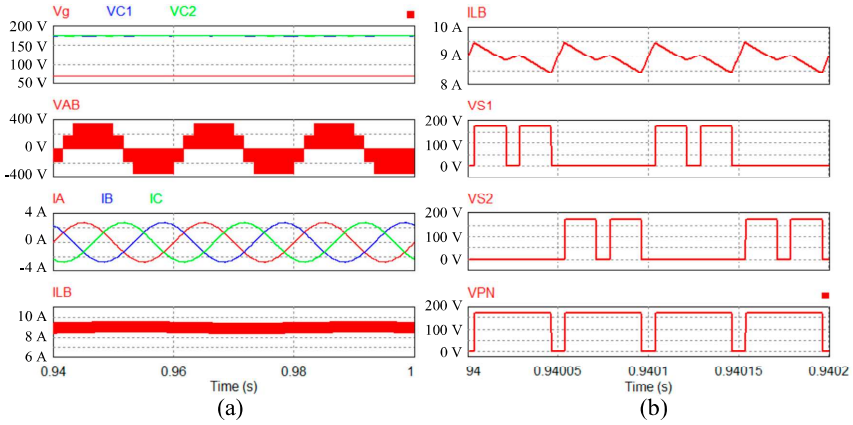

Figure 9. The simulation results of the proposed method when V_g = 70 V. From top to bottom: (**a**) input voltage (V_g), capacitor voltage (V_{C1}, V_{C2}), line-to-line voltage (V_{AB}), load current (I_A, I_B, I_C), inductor current (I_{LB}), (**b**) zoom in of inductor current (I_{LB}), impedance switch voltages (V_{S1}, V_{S2}), DC-link voltage (V_{PN}).

In both cases, the voltages on capacitors C_1 and C_2 are boosted to 180 V, as illustrated in Figures 8a and 9a. These capacitor voltages are also the voltage stresses of switches S_1 and S_2, as shown in Figures 8b and 9b. The peak value of V_{PN} is 360 V, as illustrated in Figures 8b and 9b. The maximum value inductor current ripple is approximately 1.5 A and 1 A for the cases of 200 V input voltage and 70 V input voltage, respectively. These values are obtained in ST mode, which is represented by the zero value of DC-link voltage, as presented in Figures 8b and 9b. The inductor current, I_{LB}, is also increased in NST 3, where S_1 and S_2 are turned on simultaneously. However, it is not increased faster than that of ST mode. The average inductor current is 3.4 A and 9 A for min boost and max boost control schemes, respectively. The waveform of V_{AB} is varied from −360 V and 360 V, as shown in Figures 8a and 9a. The THD value of V_{AB} is 66%. The output load current is measured as 1.95 A_{RMS}, and its THD value is 0.56% for both cases.

The comparison of CMV, V_{GO}, between the proposed scheme and strategies in [27] and [30] is shown in Figure 10. The max boost control of methods in [27,30] is applied in the simulation. The method in [30] has the largest peak-to-peak CMV value of 200 V. It can be explained by using small vectors that generate a large value of CMV in [30]. The peak-to-peak CMV values of the scheme in [27] and the proposed PWM strategy are 130 V and 120 V, respectively. The RMS CMV values of the proposed method and methods in [27,30] are 34.8 V_{RMS}, 36.5 V_{RMS}, and 56.9 V_{RMS}, respectively. It is proved that the proposed PWM strategy produces the smallest CMV.

5.2. Experimental Results

The effectiveness of the proposed PWM strategy is also validated by experiments that are obtained through a laboratory prototype, as observed in Figure 11. The parameters used for experimental verification are also the same as simulation. The IGBTs FGL40N150 are used for the S_{1X} and S_{3X} of the inverter leg as well as the active switches of the intermediate network (S_1 and S_2). The isolated voltage sensors based on LEM LV20-P sensor are used to detect the capacitor and output load voltages. The experimental results are presented in Figures 12 and 13.

For the case of a 200 V DC input source, as shown in Figure 12, the V_{C1} and V_{C2} are measured as 163 V and 170 V, respectively, as illustrated in Figure 12a. These capacitor voltages are also the voltage stresses of switches S_1 and S_2, which are 163 V and 170 V, respectively, as presented in Figure 12b. Furthermore, the max value of V_{PN} is determined as 333 V, as shown in Figure 12b. The NST mode 3 can be determined by observing the value zero of both switch S_1 and S_2 voltages, while the ST mode can be identified by observing the value zero of DC-link voltage. The inductor current is increased in both NST mode 3 and ST mode, as shown in Figure 12b. However, in ST mode, the inductor

current increment is faster than that of NST mode 3 because the voltage across the inductor is larger than that in NST mode 3, as demonstrated in Equations (1) and (4). Inductor current ripple is measured around 1.5 A. The average value of i_{LB} is measured as 3.5 A, as presented in Figure 12a. The variation of V_{AB} is from $-V_{PN}$ to $+V_{PN}$, as illustrated in Figure 12c. The output load current is measured as 1.85 A_{RMS}, and its waveform is sinusoidal. The FFT analysis for V_{AB} can be seen in Figure 12c. The first-order harmonic is also the maximum value, which is 190 V. The THD values of V_{AB} and output load current I_A are 80.5% and 2.51%.

When applying 70 V DC input source, the capacitor C_1 and C_2 voltages are 153 V and 159 V, when the coefficient D_0 is 0.85. These voltages generate 312 V of DC-link voltage, as illustrated in Figure 13b. The inductor current ripple is approximately 1.1 A, as shown in Figure 13b, and its average value is 10.4 A, as shown in Figure 13a. The output load current is 1.71 A_{RMS}. Figure 13c presents the FFT spectrum of V_{AB}, where the peak-to-peak value is 180 V at the first-order harmonic. The THD values of V_{AB} and I_A are 82.6% and 2.55%, respectively.

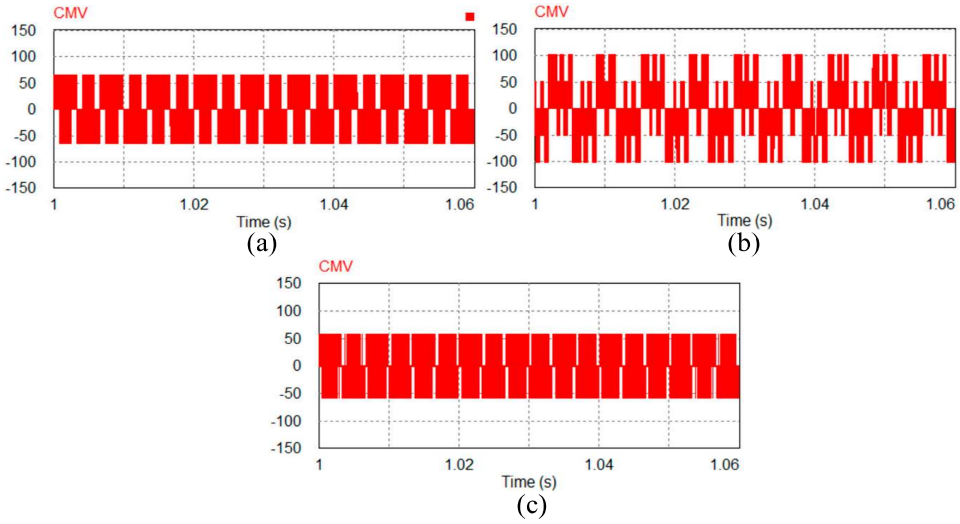

Figure 10. CMV comparison between (**a**) the method in [27], (**b**) the method in [30], and (**c**) the proposed method.

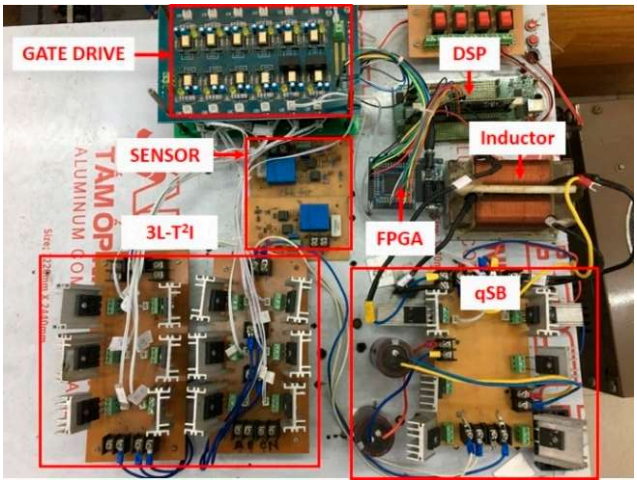

Figure 11. Experimental prototype.

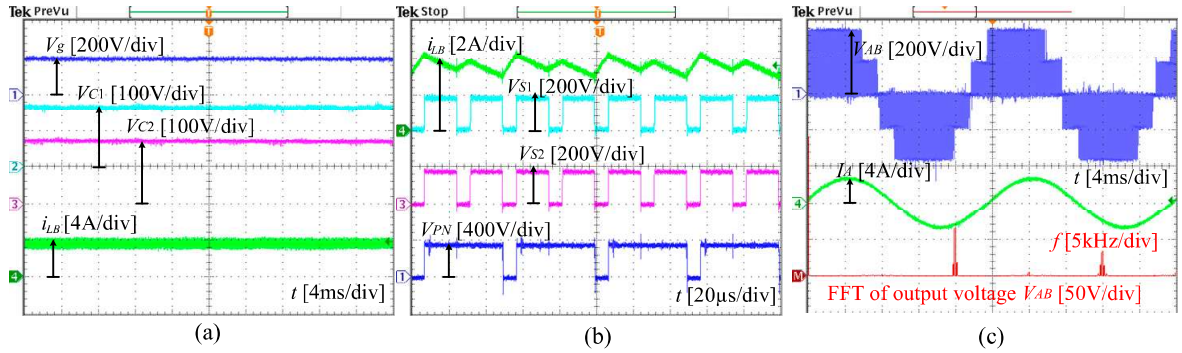

Figure 12. Experimental results of the inverter under the proposed method when V_g = 200 V. From the top to bottom: (**a**) V_g, V_{C1}, V_{C2}, and i_{LB}; (**b**) i_{LB}, V_{S1}, V_{S2}, and V_{PN}; (**c**) V_{AB}, I_A, and FFT spectrum of the output voltage V_{AB}.

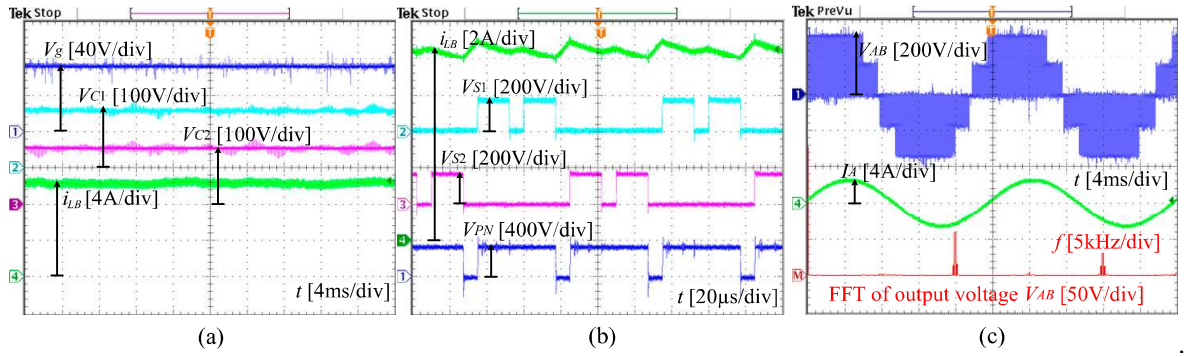

Figure 13. Experimental results of the inverter under the proposed method when V_g = 70 V. From the top to bottom: (**a**) V_g, V_{C1}, V_{C2}, and i_{LB}; (**b**) i_{LB}, V_{S1}, V_{S2}, and V_{PN}; (**c**) V_{AB}, I_A, and FFT spectrum of the output voltage V_{AB}.

The capacitor voltage balance scheme and the closed-loop control implementation for the proposed method have been conducted. The results are shown in Figures 14 and 15. The neutral voltage control is implemented in two cases: (1) the difference voltage between these capacitors v_{dif} is positive, and (2) the difference voltage between these capacitors v_{dif} is negative. In both cases, the neutral voltage balance condition is recovered after approximately 20 ms, as shown in Figure 14a,b. These results are conducted with the coefficient α of 0.3.

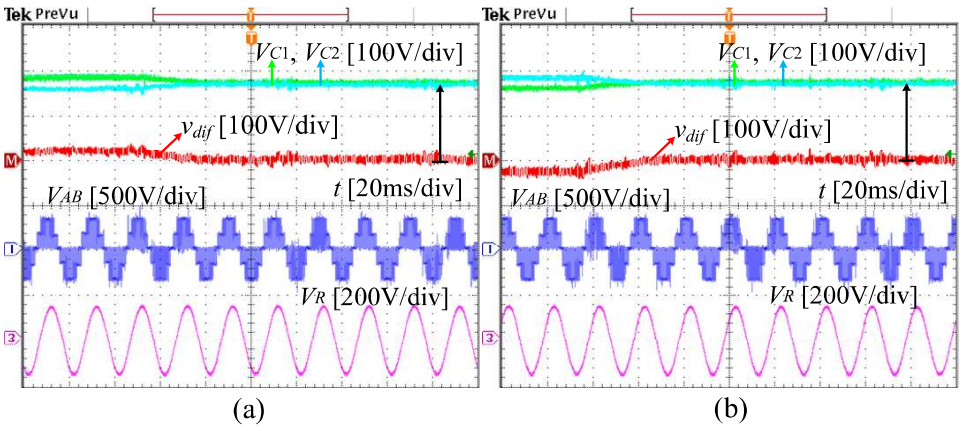

Figure 14. The experimental results for capacitor voltage balance. (**a**) $v_{dif} > 0$, (**b**) $v_{dif} < 0$.

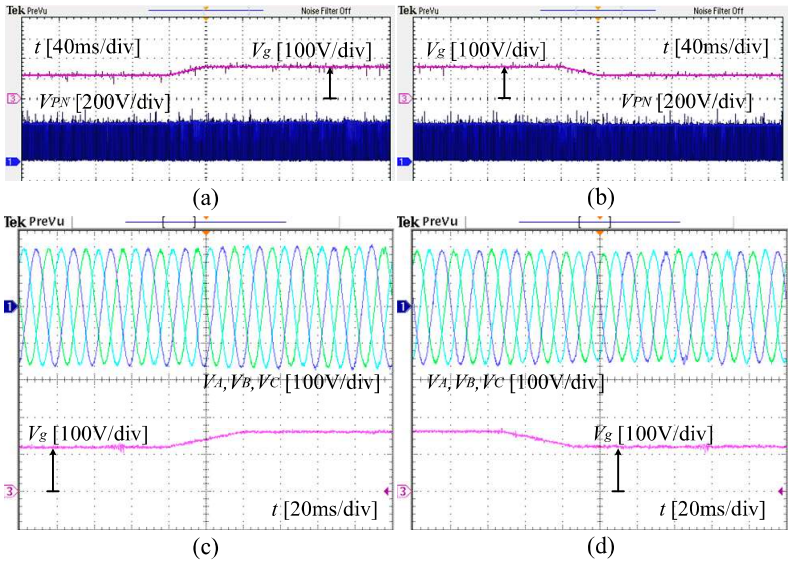

Figure 15. The experimental verification for DC-link voltage control and output load voltage control. (**a**,**c**) Input voltage increment, (**b**,**d**) input voltage decrement.

The input voltage is regulated to increase from 120 V to 160 V and decrease from 160 V to 120 V to validate the closed-loop control. In both cases, the V_{PN} is maintained at 360 V, which can be seen from Figure 15a,b. The output load voltage is kept at 110 V_{RMS} without DC input voltage variation, as presented in Figure 15c,d. In this work, the ST duty ratio D_{ST} is kept at 0.15. The modulation index is used to regulate the output load voltage and is limited to 0.85. The coefficient D_0 is utilized to control DC-link voltage, and its range is from 0.15 to 0.85.

6. Conclusions

This paper has introduced a PWM method for the 3L-qSBT^{2}I based on a third harmonic injection scheme. By applying this method, many benefits have been obtained, such as high boost factor, high voltage gain, and less voltage rating on impedance-source network devices. These advantages have been validated through some investigations, which were conducted belonging to previous publications. The details of relevant equations and designed parameter selection have been presented. Furthermore, this paper also considered the capacitor voltage unbalance problem. The time interval of NST mode, which is generated by triggering only one switch of the qSB network, has been recalculated based on the actual capacitor voltages to provide neutral voltage balance characteristics. The output voltage and DC-link voltage have been controlled by using PI controllers. The extra duty cycle of two active switches of the qSB network was adopted to regulate DC-link voltage, whereas the modulation index has been utilized to regulate the AC output voltage. The accuracy of this scheme has been validated by simulation and experimental results. With some benefits listed, such as buck-boost operation, reduced conduction loss, the low voltage stress on devices, and an easy capacitor voltage balance scheme, the 3L-qSBT^{2}I under the proposed method is suitable for PV applications where a low DC input voltage needs to be converted to a high AC output voltage with high efficiency and output quality.

Author Contributions: This article has received the same contributions from the authors. which include writing the paper and experiment implementation. This manuscript has been received agreement from all authors. This paper was a collaborative effort among all authors. D.-T.D., V.-T.T. and M.-K.N. conceived the methodology, conducted the performance tests and wrote the paper. All authors have read and agreed to the published version of the manuscript.

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A SVM Scheme for Three-Level Quasi-Switched Boost T-Type Inverter with Enhance Voltage Gain and Capacitor Voltage Balance

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***Abstract*- This paper introduces a space vector control method for the three-level quasi-switched boost T-type inverter (3L-qSBT^{2}I) which provides some benefits such as: good output voltage quality, high voltage gain, and low voltage stress on power devices. By applying corresponding P-type or N-type small vectors in switching sequence, the neutral-point voltage unbalance problem can be solved easily. The advantage of this modulation solution is that it does not require any extra calculations. The upper-shoot-through (UST) and lower-shoot-through (LST) states are utilized instead of full-shoot-through (FST), which is usually used in traditional single-stage three-level impedance source inverter, to ensure the boost capability of the inverter. These states are inserted into small vectors in order not to affect the output line-to-line voltage. Some investigations about voltage gain, diode, and switch voltage stress have been conducted to demonstrate the effectiveness of the proposed method. The experimental results are also presented to validate the accuracy of the proposed modulation method. The proposed approach has resulted in efficiency rise by 2% as compared to the conventional PWM scheme.**

***Index Terms*- Quasi-switched boost inverter, three-level inverter, impedance-source network, capacitor voltage balance, shoot-through, space vector modulation.**

I. Introduction

In recent years, Z-source (ZS), and quasi-Z-source (qZS) networks have been employed to the three-level inverters with shoot-through (ST) immunity and step up-down voltage ability [1]-[3]. Because of adopting ST state in operation which is generated by simultaneously turning on all switches of inverter, the reliability and the stability of these inverter topologies are significantly improved [4], [5]. Due to their advantages, these ZS/qZS three-level inverters were applied to photovoltaic (PV) grid-connected systems [6], [7]. To create a three-level voltage-fed buck-boost inverter, two identical ZS networks were connected in cascade form which fed by two isolated DC sources [8]-[10]. Derived from ZSI in [8]-[10], a combination of a single ZS network and the three-level inverters was investigated in [11]-[13]. Because of the symmetry of the ZS structure, a three-level voltage can be easily obtained at the output by installing a single split DC source and one extra diode. However, this structure of ZSI generates a discontinuous input current due to connecting diodes to the input source directly. In [14], a modified impedance-source network had been presented to provide the continuous input current by adding two capacitors and one extra diode to the three-level ZSI. The qZS structure was also considered incorporating with the three-level inverter [7], [15]-[17]. Because of the asymmetry of qZS network, two identical qZS are needed to create a three-level voltage at the output terminal, which is fed by a single split DC source [17]. This configuration just adopted UST and LST states to achieve buck-boost operation with a single-stage power conversion. In [7], [15], and [16], a single DC input source fed to qZS three-level inverter which utilized FST insertion instead of UST and LST insertions in [17].

In general, the ZS/qZS three-level inverters have disadvantages in using many passive components and having quite large input current ripple. Therefore, the quasi-switched boost (qSB) networks were introduced in [18] to overcome the drawbacks of ZS/qZS networks. By adding one diode and one active switch to the impedance-source network, this topology saved one inductor and one capacitor. In [19], a three-level neutral point clamped (NPC) buck-boost inverter based on qSB networks was presented. This configuration uses two identical qSB networks connecting in cascade form, which are fed by one split DC input source, to generate a three-level voltage at the output side of the inverter. For reduced device count, the studies in [20]-[22] introduced the active impedance-source networks for the three-level inverter. Many comparison studies between the impedance source inverters and traditional two-stage systems with a boost DC-DC converter followed by the voltage-source inverter have been carried out in the literature [23], [24]. Recently it was demonstrated in [25] that by combining the optimized design and control the efficiency of the three-level qZS inverter could reach 97% even with the use of generic semiconductors, which is comparable to the traditional two-stage approach.

In the impedance-source inverters, the boost factor or voltage gain are very important because they relate to component rating, output quality, conversion efficiency, etc. Therefore, the most recent studies focus on enhancing the boost factor or voltage gain [14], [20]-[22]. In the single-stage inverter, the boost operation is essentially ensured by the FST state added to zero vector [1], [4], [15], [16], [20]-[22] or UST

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and LST states added to small vectors [3], [8]-[14], [17]. In literature [14], the boost factor is enhancing to twice of conventional impedance-source inverters in [1], [3], [4], [7]-[13], [15]-[17] by adopting UST and LST insertions for the modified ZSI. In comparison to [14], the same boost factor is obtained in the studies in [20]-[22] with smaller number of passive components and adopting FST state. Comparing to [20], [21], the topology in [22] can achieve the same boost factor with reduced component count. However, the inductor current profile of [20], [21] is better than that of [22].

Another problem of the three-level inverter is the neutral voltage unbalancing issue. To solve this problem, the virtual space vector modulation is considered as a sensorless solution to ensure the balancing condition [26]-[29]. The main idea of these works is generating zero value of average value of neutral-point current in any switching period. However, the effects of intermediate network as well as the buck-boost operation are not carefully considered in these studies. Moreover, it is difficult to apply this solution to the single-stage buck-boost inverter. It should be noted that the sensor is necessary for DC-link voltage and output voltage regulations regardless of whether the inverter provides capacitor voltage balancing or not. For example, the work in [28] uses the sensorless method in [26] to balance the capacitor voltages, but the sensors are still used to control the DC-link voltage.

For the single-stage buck-boost inverter, the traditional solutions to solve this issue can be classified as: 1) using corresponding topology [22] or 2) utilizing PWM control method [13]-[15], [20]. For the first method in [22], the FST state is utilized for balancing capacitor voltages by connecting these capacitors in parallel. This solution can fix the difference between two capacitor voltages to a constant value. Nevertheless, this value is still large which is affected by the parasitic of the circuit. Regarding the second solution, in [20], this problem can be handled by adjusting the extra duty ratios of switches of impedance-source network. As mentioned in [20], the difference between duty ratios of intermediate network switches is obtained by the PID controller which is fed by the difference between actual values of two capacitor voltages. However, this work causes the boost factor effect. Moreover, the time interval for balancing recovery time is still large. In literature [13], the time intervals of P-type and N-type of small vectors have been changed to balance the capacitor voltages, which leads to change the time interval of UST and LST states. The result is that the boost factor is affected like [20]. In this solution, the faster speed of neutral point voltage balance causes the more boost factor oscillation. This is also the main drawback of the neutral voltage balance solution of the work in [14], where the duty ratios of UST and LST states are selected to adjust the speed of balancing. The solution in [15] can handle this drawback by adding one more P-type or N-type small vector into original switching sequence mentioned in [16]. The buck-boost capability is ensured by FST state which does not affect by extra small vector. However, the complexity dwell-time calculation of extra small vector is the main disadvantage of this work.

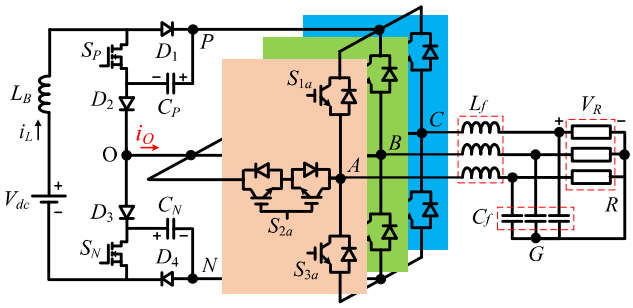

Fig. 1. Topology of 3L-qSBT^{2}I.

To summarize, these studies of impedance-source inverters have some drawbacks as: 1) small boost factor and voltage gain, 2) complexity neutral voltage balance scheme, and 3) affecting the boost factor when obtaining balancing condition. This paper introduces a new SVM strategy for 3L-qSBT^{2}I to improve the voltage gain of the inverter, in which the small vectors are considered to create UST and LST states instead of FST state. Consequently, this strategy provides the advantage of producing low voltage stress on power devices. Furthermore, this paper presents a control scheme to solve the capacitor voltage unbalance problem by selecting the corresponding small vectors based on actual capacitor voltages without requiring any extra calculations, which does not cause the boost factor effect. The comparison between the proposed technique and the existing PWM methods is conducted to demonstrate the effectiveness of the proposed SVM strategy. An inverter prototype is built in laboratory to validate the effectiveness of the proposed SVM scheme. The rest of this paper is classified as follows. In section II, the topology of 3L-qSBT^{2}I is described. Section III presents the proposed SVM strategy with enhancing voltage gain and neutral voltage balancing scheme. In section IV, the comparison study between the proposed method and the conventional method is carried out. Section V shows the experimental results to verify the proposed scheme. Section VI concludes the paper.

II. Three-Level Quasi Switched Boost T-Type Inverter (3L-qSBT^{2}I) Topology

Fig. 1 shows the 3L-qSBT^{2}I [20] which consists of an impedance-source network and a conventional three-level T-type inverter (3L-T^{2}I). Similar to other three-level inverters, this topology enables to produce a three-level voltage at the output terminal. The positive point "*P*", mid-point "*O*" and negative point "*N*" of the intermediate network are connected to the load by triggering S_{1x}, S_{2x}, and S_{3x} (x = *a, b, c*), respectively. The result is that the output pole voltage achieves $+V_{PN}/2$, 0, and $-V_{PN}/2$. The amplitude of the high-frequency harmonic of the output voltage is mitigated by installing a three-phase low-pass filter before the output load. The neutral-point current i_O is defined as the current going from the mid-point "*O*" to inverter branch, as shown in Fig. 1.

Like [20], the 3L-qSBT^{2}I has two operating modes in one switching period: non-ST (NST) and ST modes. The NST mode is controlled by triggered both switches of impedance-source which consists of NST1, NST2, NST3, and NST4, as illustrated in Fig. 2(a), 2(b), 2(c), and 2(d).

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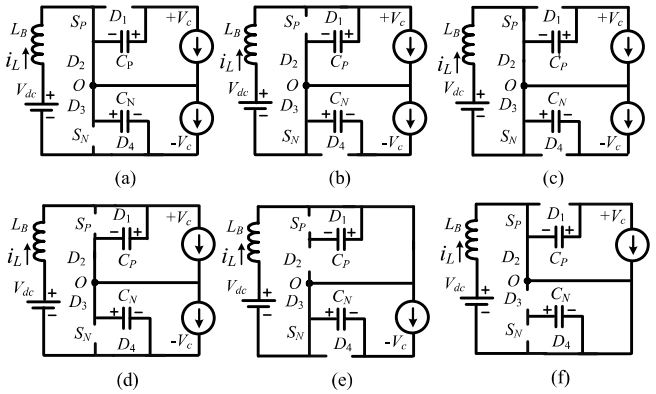

Fig. 2. Operating modes of 3L-qSBT^{2}I. (a) NST1, (b) NST2, (c) NST3, (d) NST4, (e) UST, and (f) LST.

TABLE I
SWITCHING STATES OF 3L-QSBT^{2}I ($X = A, B, C$)

Mode	ON Switch	ON Diode	V_{LB}	V_{xO}
NST1	S_P	D_2, D_3, D_4	V_{dc}-V_{CN}	$+V_{PN}/2$, 0, $-V_{PN}/2$
NST2	S_N	D_1, D_2, D_3	V_{dc}-V_{CP}	$+V_{PN}/2$, 0, $-V_{PN}/2$
NST3	S_P, S_N	D_2, D_3	V_{dc}	$+V_{PN}/2$, 0, $-V_{PN}/2$
	S_{1x}			$+V_{PN}/2$
NST4	S_{2x}	D_1, D_2, D_3, D_4	V_{dc}-V_{CP}-V_{CN}	0
	S_{3x}			$-V_{PN}/2$
UST	S_{1x}, S_{2x}, S_N	D_1, D_3	V_{dc}	0 *or* $-V_{PN}/2$
LST	S_{2x}, S_{3x}, S_P	D_2, D_4	V_{dc}	0 *or* $+V_{PN}/2$

The ST mode is achieved by adding the ST state into the N-type and P-type small vectors to create the UST and LST modes, respectively. The value of $+V_{PN}/2$ is generated at the output side of qSB network, as shown in Figs. 2(e) and 2(f). In general, assume that the small vectors used to generate the UST and LST states are "*OON*" and "*POO*", respectively. The ST insertion is detailed as follows.

Like other conventional 3L-T^{2}I, to generate the "*OON*" state at the output of inverter side, the switches S_{2a}, S_{2b} and S_{3c} are turned on at the same time. Consequently, the capacitor C_N is needed to guarantee the "O" and "*N*" states at the output terminals, whereas the capacitor C_P does not generate any active states at output. Therefore, it does not affect the output voltage when disconnecting the upper capacitor C_P to the power circuit. To reach the UST state, this configuration simultaneously turns on the high side switch of the phase operating at the "*O*" state with switch S_N to store energy for input inductor, as shown in Fig. 2(e). Based on this analysis, switches S_{1a} or S_{1b} and S_N are triggered on at the same time to switches S_{2a}, S_{2b} and S_{3c}. As a result, the diode D_2 is reserved bias which leads to disconnect the capacitor C_P to the inverter circuit. The inductor L_B stores energy from the DC source without affecting the output voltage, as shown in Fig. 2(e).

Like UST mode, the LST mode is achieved by turning on switches S_{3b} or S_{3c} and S_P at the same time to switches S_{1a}, S_{2b}, and S_{2c} when the inverter produces the vector "*POO*" at the output. Consequently, diodes D_2 and D_4 are forward-bias whereas diodes D_1 and D_3 are reversed-bias. Capacitor C_P provides energy to the load while capacitor C_N is disconnected to the main circuit, as shown in Fig. 2(f). Inductor L_B is stored energy and its voltage is expressed as Table I.

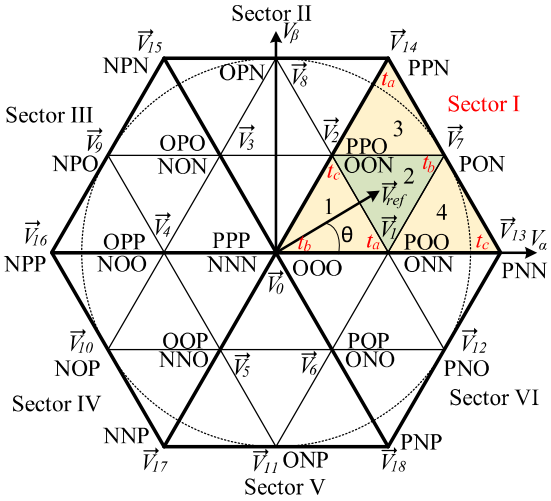

Fig. 3. Space vector diagram of the proposed strategy.

TABLE II
DWELL-TIME OF SECTOR I

Region	t_a	t_b	t_c
1	$2MT_s\sin(\pi/3-\Theta)$	$T_s-2MT_s\sin(\pi/3+\Theta)$	$2MT_s\sin(\Theta)$
2	$T_s-2MT_s\sin(\Theta)$	$2MT_s\sin(\pi/3+\Theta)-T_s$	$T_s-2MT_s\sin(\pi/3-\Theta)$
3	$2MT_s\sin(\Theta)-T_s$	$2MT_s\sin(\pi/3-\Theta)$	$2T_s-2MT_s\sin(\pi/3+\Theta)$
4	$2T_s-2MT_s\sin(\pi/3+\Theta)$	$2MT_s\sin(\Theta)$	$2MT_s\sin(\pi/3-\Theta)-T_s$

III. PROPOSED SVM METHOD

Fig. 3 shows the space vector diagram of the proposed method for the 3L-qSBT^{2}I. As illustrated in Fig. 3, there are six sectors (I-VI) where each sector is divided into four separate regions. The proposed method synthesizes the reference vector by three nearest vectors. The detail of dwell-time calculations, ST insertion, the neutral-point voltage balance strategy, steady-state analysis, and the overall control scheme are presented in this section. As an example, region 2 of sector I is considered in analysis of the proposed strategy.

A. Dwell-Time Calculation

In general, assume that the reference vector locates in sector I and region 2. As a result, the vectors $\vec{V}_1$, $\vec{V}_2$, and $\vec{V}_7$ are adopted to generate the reference vector. The relationship between these vectors is expressed as:

$$\begin{cases} \vec{V}_{ref}.T_s = \vec{V}_1.t_a + \vec{V}_7.t_b + \vec{V}_2.t_c \\ T_s = t_a + t_b + t_c \end{cases} \quad (1)$$

where $\vec{V}_{ref}$, $\vec{V}_1$, $\vec{V}_2$, and $\vec{V}_7$ are the reference vector, small vectors, and medium vector, respectively. T_s is the switching period of the inverter. t_a, t_b, and t_c are the on-times of $\vec{V}_1$, $\vec{V}_7$ and $\vec{V}_2$, respectively.

The reference vector ($\vec{V}_{ref}$), small vectors ($\vec{V}_1$, $\vec{V}_2$), and medium vector ($\vec{V}_7$) are identified as:

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$$\begin{cases} \vec{V}_{ref} = 1/\sqrt{3}.M.V_{PN}.e^{j\theta} \\ \vec{V}_1 = 1/3.V_{PN}.e^{j0} \\ \vec{V}_2 = 1/3.V_{PN}.e^{j\pi/3} \\ \vec{V}_7 = 1/\sqrt{3}.V_{PN}.e^{j\pi/6} \end{cases} \quad (2)$$

where M is the modulation index and V_{PN} is the peak value of DC-link voltage.

Based on equation (1) and (2), the dwell-times of these vectors can be identified as:

$$\begin{cases} t_a = T_s - 2MT_s \sin(\theta) \\ t_b = 2MT_s \sin(\theta + \pi/3) - T_s \\ t_c = T_s - 2MT_s \sin(\pi/3 - \theta) \end{cases} \quad (3)$$

The dwell-times calculation for other regions of this sector is detailed in Table II.

B. Switching Sequence Selection for Neutral Voltage Balance

As shown in Fig. 3, all small vectors always have redundant vectors which are P-type and N-type forms of small vectors. Considering each small vector, these types generate the same output voltage, whereas each type makes the upper and lower capacitor voltages changing differently.

Considering small vector $\vec{V}_1$ as an example, this vector has two equivalent vectors: [*POO*] and [*ONN*] as shown in Fig. 3. In NST4, the currents through two capacitors and neutral-point "O" when adopting the P-type and N-type of small vector $\vec{V}_1$ are expressed in Fig. 4. When the P-type of $\vec{V}_1$ is adopted, the upper (C_P) and lower (C_N) capacitors are charged by the charger currents as ($i_L - i_{load}$) and i_L, as shown in Fig. 4(a). Assume that, capacitances of C_P and C_N are the same, the capacitor C_N voltage is increased faster than C_P voltage due to having larger charger current. In simply, the neutral-point current i_O is negative (i_O = -i_{load}). In this case, it makes the capacitor C_P voltage tends to be smaller than capacitor C_N voltage, as mentioned in [26]. Therefore, by adopting only this P-type of small vector, the capacitor C_N voltage will be larger than capacitor C_P voltage. It is also true for another P-type of small vectors. Similarly, for N-type of small vector shown in Fig. 4(b), the currents of capacitors C_P, C_N, and neutral-point voltage i_O are respectively determined as i_L, $i_L - i_{load}$, and i_{load}, which makes the capacitor C_P voltage tend to be larger than capacitor C_N voltage. This analysis is also true for other N-type of small vectors and other operating modes.

Based on above analysis, to balance neutral-point voltage when the upper capacitor voltage is larger than the lower capacitor voltage, the P-type small vectors are adopted in switching sequence instead of N-type small vectors and vice versa. Therefore, the switching sequence of region 2 of sector I is selected as: 1) when capacitor C_N voltage (V_{CN}) is larger than capacitor C_P voltage (V_{CP}), the switching sequence is [*ONN*]-[*OON*]-[*PON*]-[*OON*]-[*ONN*] and return; 2) when V_{CN} is less than V_{CP}, the switching sequence is [*PPO*]-*POO*]-[*PON*]-[*POO*]-[*PPO*] and return. As a result, the capacitor C_P voltage in case 1 is increased, while the capacitor C_N voltage is decreased as illustrated in Fig. 5(a). Opposite to case 1, the capacitor C_P voltage is decreased over switching period,

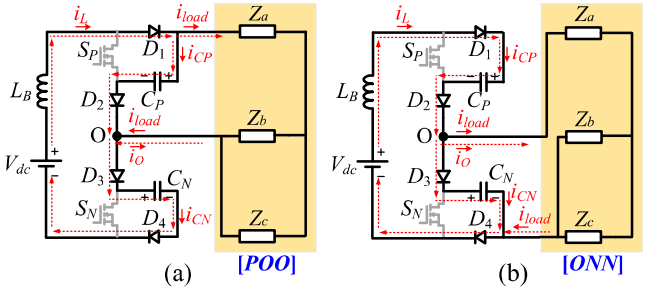

Fig. 4. The effect of small vectors to capacitor voltage balance in NST4. (a) P-type small vector [*POO*], (b) N-type small vector [*ONN*].

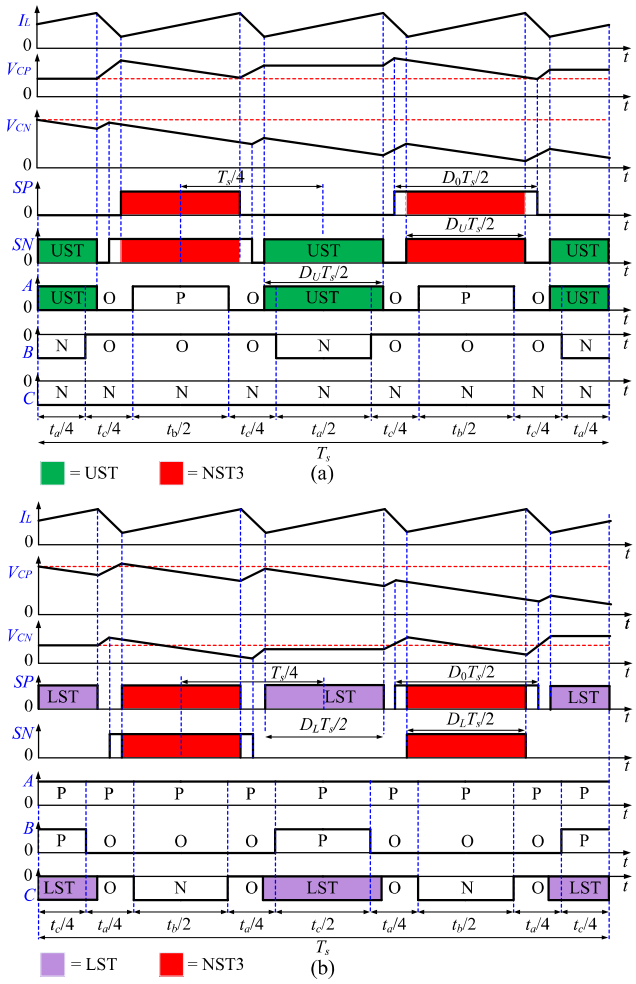

Fig. 5. Switching sequence in sector I, region 2 and control signals of S_P and S_N. (a) $V_{CP} < V_{CN}$, (b) $V_{CP} > V_{CN}$.

whereas the capacitor C_N voltage is increased as shown in Fig. 5(b). Noted that although the proposed method also adopts large vector and medium vector in switching sequence, it does not affect the neutral voltage balance operation. As mention in [26], because the large vector generates the zero value at neutral current i_O, it does not generate capacitor unbalance, while adopting the medium vector can cause capacitor unbalance. However, it can be compensated by adopting corresponding small vector [15].

To guarantee the buck-boost operation, the UST and LST states are considered to respectively insert to N-type and P-type small vectors in case 1 and case 2, as shown in Fig. 5(a) and 5(b). In fact, the UST state in case 1 can be inserted to phase A and phase B for vector [*OON*] and only phase A for vector [*ONN*], as detailed in section II. However, to minimize the number of communications, the UST state is only added to phase A. The same as case 1, the LST state is added to phase C to minimize the switching loss. It should be noted that the UST and LST insertions do not affect the output voltage, it means that the phase selected to add UST or LST states still produces "*O*" state at output terminal.

By applying the same way to other regions and other sectors, the switching sequence, UST and LST state insertion can be determined easily. For instant, the capacitor voltage balance in zone 3 of sector I is achieved by adopting properly small vector [PPO] or [OON] based on the actual values of capacitor C_P and C_N voltages. For example, when the capacitor C_P voltage is larger than the capacitor C_N voltage, vector [PPO] is adopted to decrease the capacitor C_P voltage and increase the C_N voltage. Then, the switching sequence is [PPO]-[PPN]-[PON]-[PPN]-[PPO] and return, the LST state is inserted within vector [PPO]. When the capacitor C_P voltage is smaller than capacitor C_N voltage, vector [OON] is adopted to increase the C_P voltage and decrease the C_N voltage, in which the switching sequence is [OON]-[PON]-[PPN]-[PON]-[OON] and return. The UST state is added to vector [OON].

To achieve high voltage gain and low inductor current ripple, the NST3 generated by turning on both S_P and S_N switches is created with some characteristics as: 1) its time interval is equal to UST or LST state time intervals, 2) this signal is shifted as 90 degree to UST state or LST state. Furthermore, extra duty ratio D_0 is also applied for S_P and S_N switches. The detail is presented in Fig. 5.

C. Steady-State Analysis of 3L-qSBT²I with Proposed SVM Method

In two forms of switching sequences shown in Fig. 5, the total time interval of N-type small vectors equals to P-type small vectors. Therefore, in order not to affect the boost factor, this scheme generates the same time intervals of UST and LST state which are inserted into N-type and P-type small vectors, respectively. In general, the duty ratio of UST state (D_U) and duty ratio of LST state (D_L) are called as D_{ST}.

Based on the operating principle presented in section II and the control signals of the proposed SVM scheme presented in Fig. 5, the time interval of NST1 and NST2 is $(D_0 - D_{ST})T_S/2$, in each switching period (T_s). The time interval of NST3 and the ST mode are $D_{ST}T_S$. As a result, the rest time interval of T_S is the total time interval of NST4, which is $(1 - D_0 - D_{ST})T_S$. Assume that the capacitance of C_P and C_N are large enough to ensure that these capacitor voltages are constant, and ($V_{CP} = V_{CN} = V_C$). Because the average value of inductor voltage is zero, these capacitor voltages can be calculated as:

$$V_C = V_{CP} = V_{CN} = V_{dc} / \left(2 - 3D_{ST} - D_0\right) \tag{4}$$

where V_{CP} and V_{CN} are the capacitor voltages of C_P and C_N, respectively; V_{dc} is the DC input voltage; D_{ST} is the ST duty ratio; and D_0 is the duty ratio of switches S_P and S_N.

The boost factor (B) of the inverter is identified as:

$$B = V_{PN} / V_{dc} = 2 \times V_C / V_{dc} = 2 / (2 - 3D_{ST} - D_0) \tag{5}$$

The peak-value of the first-order harmonic of output phase voltage ($V_{x,peak}$) is calculated as:

$$V_{x,peak} = \frac{2}{\sqrt{3}} M V_C = \frac{2}{\sqrt{3}} \cdot \frac{M \cdot V_{dc}}{2 - 3D_{ST} - D_0} \tag{6}$$

The voltage gain (G) of the inverter can be expressed as:

$$G = \frac{V_{x,peak}}{V_{dc}/2} = \frac{4}{\sqrt{3}} \cdot \frac{M}{2 - 3D_{ST} - D_0} \tag{7}$$

The UST and LST states must be inserting within small vectors. Based on the dwell-time calculations of small vectors in section A, for example, for section I shown in Table II, the minimum value of the total time interval of small vectors in one switching period (T_S) is $2(1 - M)T_s$, during operation. Therefore, the relationship between ST duty ratio D_{ST} and modulation index M is expressed as:

$$D_{ST} \le 2 \cdot (1 - M) \tag{8}$$

In previous studies for single-stage three-level inverter, the maximum value of the ST duty ratio is limited as $(1 - M)$ [13]-[15], [20], [22]. However, the ST duty ratio of this proposed method is extended into twice that of the previous methods for the same modulation index. Therefore, the voltage gain is significantly enhanced.

The duty ratio D_0 and the ST duty ratio D_{ST} must be [20]:

$$D_{ST} \le D_0 \le 1 - D_{ST} \tag{9}$$

The variation of coefficient D_0 causes the variation of voltage gain G, as presented in equation (7). When applying the values D_{ST} and $(1–D_{ST})$ for the coefficient D_0, the proposed method achieves the minimum voltage gain and maximum voltage gain, respectively. To obtain the possible maximum boost factor, the ST duty ratio is set as $2(1 - M)$, which is based on formula (8). Thus, the minimum and maximum value of G are respectively expressed as:

$$G_{\min} = \frac{2M/\sqrt{3}}{4M - 3} \quad \text{and} \quad G_{\max} = \frac{4M/\sqrt{3}}{4M - 3} \tag{10}$$

D. Implementation of the Overall Control Scheme

The overall control scheme of the proposed SVM method is divided into two sections, which are DC-link voltage control and neutral voltage balance implementation, as shown in Fig. 6. Based on (5), the DC-link voltage can be regulated through two coefficients which are ST duty ratio D_{ST} and extra duty ratio D_0. Similar to [20], the DC-link voltage regulation is obtained by controlling coefficient D_0, whereas the ST duty ratio are fixed based on the range of input voltage which can be calculated by applying the range of D_0 from (9). By this way, the value of D_0 can be obtained by PI controller to minimize error between the actual DC-link voltage V_{PN} and desired DC-link voltage V_{PN}^*, as shown in Fig. 6. Noted that because the DC-link voltage waveform is a pulse wave, it is impossible to feedback the DC-link voltage to controller

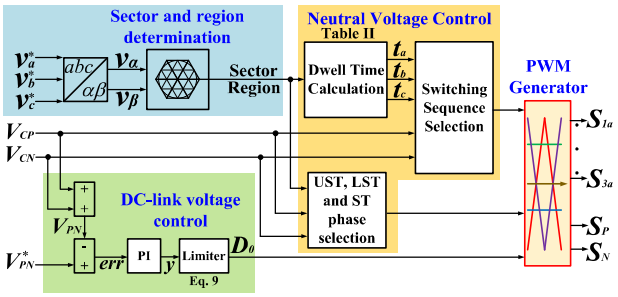

Fig. 6. Algorithm of capacitor voltage balancer and DC-link voltage control.

directly. Instead of that, this DC-link voltage can be calculated through capacitor voltages V_{CP} and V_{CN} by summing these capacitor voltages. The output of PI controller is limited by (9) in order not to affect the operating modes of the inverter.

The desired AC output voltage is used to calculate the reference vector $\vec{V}_{ref}$ (V_α, V_β) by using *abc*-$\alpha\beta$ transformation, as illustrated in Fig. 6. Then, the location of the reference vector is determined. The location of $\vec{V}_{ref}$ is used to determine which three nearest vectors are used to synthesize the reference vector and their dwell-times, as mention in section III.A. The actual values of capacitor voltages V_{CP} and V_{CN} are utilized to generate switching sequence and UST and LST states to balance the neutral voltage, as detailed in section III.B. Finally, the PWM control signals of inverter switches are generated based on these calculations.

IV. Comparison with Other PWM Techniques for Three-Level Buck-Boost Inverters

In order to figure out the superiority of the proposed SVM strategy, some single-stage three-level inverters and methods are used to make comparisons with the proposed method. They are the three-level ZSI (3L-ZSI) and modified ZSI (MZSI) in [13], [14], the three-level qZSI in [15], the 3L-qSBT^{2}I introduced in [20], [22]. Among these studies, the PWM control method in [13], [14] and the proposed method use the UST and LST insertions instead of FST insertion like [15], [20], [22]. In literature [13], the duty ratio of UST and LST represented by D_{ST} in Table III are equal to the duty ratio of the FST in other methods if they use the same modulation index. To achieve the same modulation index for all schemes, the third harmonic injection is considered to replace the sine-PWM method introduced in [14] and [20]. It is worth noting that this replacement does not affect the operation of the MZSI in [14] and 3L-qSBT^{2}I in [20]. Table III expresses the overall comparison between the proposed method to other structures and PWM strategies.

For a fair comparison, the voltage gain and component rating of the converter with the proposed method and others have been considered. In Fig. 7(a), the voltage gain of these schemes has been determined with the same modulation index. It can be seen that the proposed method produces the highest voltage gain over the schemes in [13] – [22]. This superiority can be explained by adopting larger ST duty ratio for the same modulation index. As detailed in (8), the proposed method limits the ST duty ratio as 2(1-M), whereas which ones is just (1-M) for the studies in [13] – [22]. Having higher voltage gain makes the proposed SVM method requires less ST duty ratio D_{ST} to ensure the same voltage gain. For example, assume that the proposed method needs the value k for ST duty ratio D_{ST} to generate the desired voltage gain when applying the maximum voltage gain. It must be $(1 + k) / 3$ for ZSI in [13] and qZSI in [15], and $1.5k / (1 + k)$ for MZSI in [14], and qSBI in [20] and [22] with maximum voltage gain in [20]. It can be observed that the ST duty ratio of the proposed SVM scheme is smallest in term of $k < 0.5$. As a result, the smaller boost factor and DC-link voltage are required to reach

TABLE III
COMPARISON BETWEEN PROPOSED METHOD WITH OTHER CONFIGURATIONS AND PWM METHODS

	3L-ZSI/1-LC [13]	3L-MZSI [14]	3L-qZSI/2-LC [15]	3L-qSBI/1-L [22]	3L-qSBI/1-L [20]	Proposed Method
ST duty ratio, D_{ST}	$1 - M$	$1 - M$	$1 - M$	$1 - M$	$1 - M$	$2(1 - M)$
Boost factor, B	$1/(1 - 2D_{ST})$	$2/(1 - 2D_{ST})$	$1/(1 - 2D_{ST})$	$2/(1 - 2D_{ST})$	$2/(3 - 2D_{ST} - D_0)$	$2/(3 - 2D_{ST} - D_0)$
Voltage gain, G	$1.15 \cdot MB$	$1.15 \cdot MB$	$1.15 \cdot MB$	$1.15 \cdot MB$	$1.15 \cdot MB$	$1.15 \cdot M B$
Capacitor voltage stress, V_c/V_{dc}	$(1 - D_{ST})B$	$D_{ST} \cdot B/2$; $(1 - D_{ST})B/2$	$D_{ST} \cdot B/2$; $(1 - D_{ST})B/2$	$B/2$	$B/2$	$B/2$
Diode voltage stress, V_D/V_{dc}	$B/2$	$B/2$	$B/2$	$B/2$	$B/2$	$B/2$
Switch voltage stress, V_S/V_{dc}	NA	NA	NA	$B/2$	$B/2$	$B/2$
Inductors	2	2	4	1	1	1
Capacitors	2	4	4	2	2	2
Diodes	2	3	2	2	4	4
Impedance Switches	NA	NA	NA	1	2	2
Input current ripple	Very High	High	High	High	Small	Small
Input current	Discontinuous	Continuous	Continuous	Continuous	Continuous	Continuous
Capacitor voltage balance	Complexity	Complexity	Complexity	Simple	Simple	Simple
Output quality	High	High	Low	Low	Low	High

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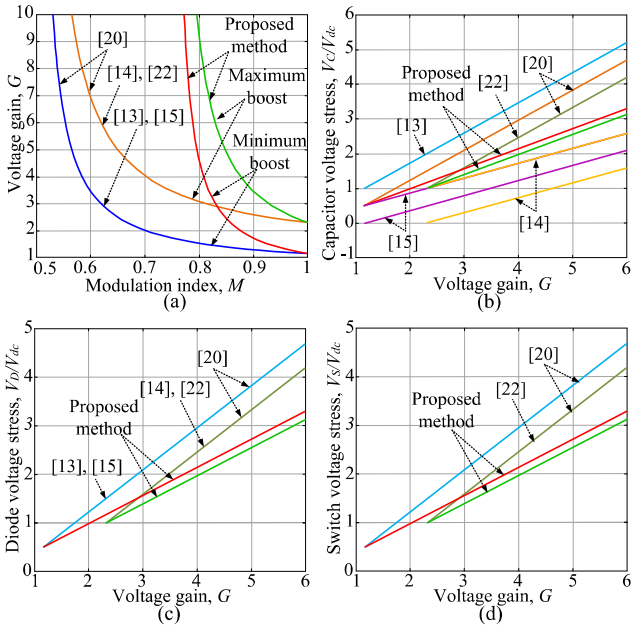

Fig. 7. Comparison between proposed method and others. (a) M vs. G, (b) G vs. capacitor voltage stress, (c) G vs. diode voltage stress, and (d) G vs. switch voltage stress.

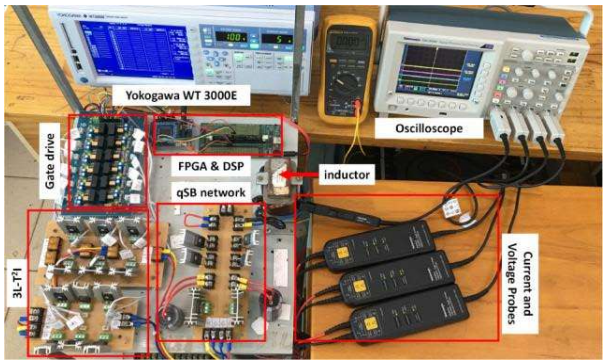

Fig. 8. The photo of experiment prototype.

TABLE IV
EXPERIMENTAL PARAMETER

Parameter/ Components		Values
DC input voltage	V_{dc}	70 V – 210 V
AC output voltage	$V_{x,RMS}$	110 V_{RMS}
Output frequency	f_0	50 Hz
Switching frequency	f_s	10 kHz
Input inductor	L_B	3 mH/20 A
Capacitors	C_P and C_N	1 mF/400 V
LC filter	L_f and C_f	3 mH and 10 μF
Resistor load	R	56Ω

the same output voltage, when utilizing the proposed SVM method. As a result, the voltage stresses on capacitors, diodes and switches are significantly reduced as detailed in follows.

Because the voltage stress of diodes in these topologies and switches of qSBI in [20]-[22] are a half of DC-link voltage as shown in Table III, the proposed SVM method generates less component rating on diodes and switches, as shown in Figs. 7(c) and 7(d), for the same voltage gain. For capacitor voltage stress, the MZSI in [14] and qZSI in [15] are proved superior due to using a larger number of capacitors, which are four capacitors for each topology, as illustrated in Table III. Among the rest topologies and schemes, the proposed method also has superior in capacitor voltage stress, as shown in Fig. 7(b). Consequently, the main contribution of the introduced SVM method is to improve the voltage gain and decrease the component rating compared to other buck-boost three-level inverters and schemes.

V. EXPERIMENTAL VERIFICATION

The accuracy of the proposed SVM method is further verified through experiments by applying the 1 kVA laboratory prototype as shown in Fig. 8. The parameters utilized for experiments are listed in Table IV. This experimental prototype is controlled by DSP F28335 microcontroller and FPGA Cyclone II EP2C5T144C8. The switches used for the impedance network are MOSFET 6R045A. The IGBTs FGL40N120D are applied for the 3L-T^2I switches. These MOSFETs and IGBTs are driven by isolated IC TLP250. The diodes used in experiments are DSEI60-12A.

The experiments are conducted with the range of DC input voltage from 70 V to 210 V. These experiments set the modulation index as 0.93 for input voltage as 210 V and 0.8616 for input voltage as 70 V. With the low-pass filter parameter listed in Table IV, the cut-off frequency is set to 1kHz, approximately. To obtain a boost factor as high as possible, the ST duty ratio (D_{ST}) is set to 0.14 and 0.2768 when the input voltage is 210 V and 70 V, respectively. The duty ratio of impedance switches S_P and S_N (D_0) is 0.14 and 0.7232. The result is the output voltage is mathematically maintained as 110V_{RMS} without the variation of DC input voltage. The work in [20] is considered comparing with the proposed SVM method. Due to using the same topology, all prototype parameters utilized for the introduced method are applied for the scheme in [20]. For the range of input voltage from 70 V to 210 V, the modulation index M, ST duty ratio D_{ST} and extra duty ratio D_0 of [20] are 0.815, 0.185 and 0.185 for the case of 210 V, and 0.67, 0.33 and 0.67 for 70 V, respectively. Figs. 9 and 10 show the experimental results for both methods in two cases of 210 V and 70 V input voltages, respectively. The Figs. 9(a), 9(c), 10(a) and 10(c) are conducted for the method in [20], the rest figures are the experimental results under the proposed method. Table V shows the comparison of the capacitor voltage stress and THD values of output voltage and current between the proposed method and method in [20].

In case 1, the capacitor C_P and C_N voltages are respectively booted to 144 V and 143 V from 210 V input voltage for the proposed method as shown in Fig. 9(e), while, they are 161 V and 159 V for the work in [20], which can be seen from the peak-value of voltages across switches S_P and S_N in Fig. 9(c), and listed in Table V. It demonstrates that the proposed method produces less voltage stress on capacitor than method in [20]. Because the voltage stress on power devices of this topology like diodes and switches is equal to capacitor

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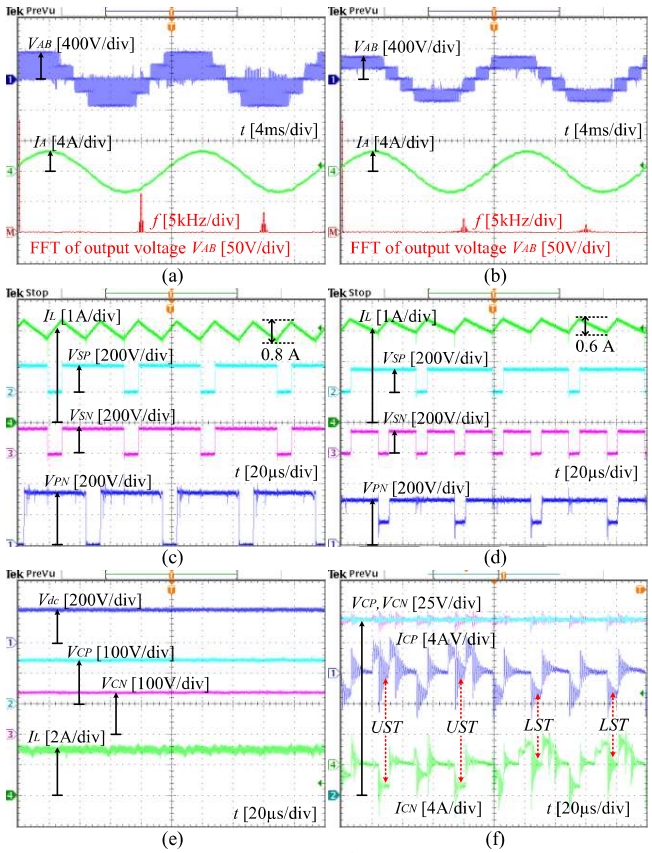

Fig. 9. Experimental results of 3L-qSBT^{2}I with proposed SWM method and method in [20] when V_{dc} = 210 V: (a), (c) the method in [20], (b), (d), (e), (f) the proposed SVM method.

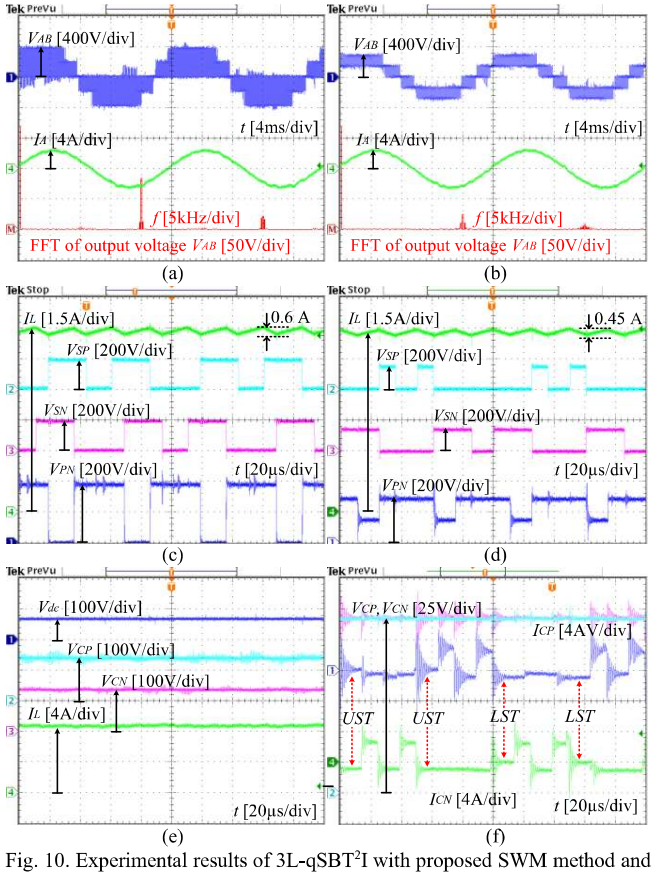

Fig. 10. Experimental results of 3L-qSBT^{2}I with proposed SWM method and method in [20] when V_{dc} = 70 V: (a), (c) the method in [20], (b), (d), (e), (f) the proposed SVM method.

voltages, the proposed method has a good voltage stress on power devices than the work in [20] as presented in Figs. 9(c) and 9(d). The DC-link voltage for method in [20] and the proposed SVM method are 320 V and 287 V, as illustrated in Figs. 9(c) and 9(d), respectively. Due to having larger DC-link voltage, the method in [20] has a higher voltage stress on switches of 3L-T^{2}I branch.

The inductor peak-to-peak current ripple of the method in [20] is larger than the proposed method which are respectively measured as 0.8 A and 0.6 A. The output line-line voltage quality of the method in [20] is worse than the introduced method, as shown in Figs. 9(a) and 9(b). The amplitudes of high frequency harmonics of [20] are larger than the proposed method, which makes the THD value of output voltage of [20] larger. The THD values are calculated as 65.9% for [20] and 47.8% for the proposed method. The result shows that the THD value of output load current of [20] is also worse at 2.55% as shown in Table V, while it is 1.76% for the proposed method. The output load currents of these methods are the same which are 1.84 A_{RMS} approximately. The inductor current of the proposed method is shown in Fig. 9(e) and measured as 2.83 A for average value.

All advantages of the proposed method over the method in [20] for the case of 210 V input voltage mentioned above are also applied for the case of 70 V input voltage. The comparison results are presented in Fig. 10 and Table V. For the proposed method, the average value of inductor and RMS value of output load currents are measured as 8.36 A and 1.72 A_{RMS} as illustrated in Figs. 10(e) and 10(b).

TABLE V
COMPARISON BETWEEN METHOD IN [20] AND PROPOSED METHOD

	V_{dc} = 210 V		V_{dc} = 70 V	
	Method in [20]	Proposed SVM method	Method in [20]	Proposed SVM method
Capacitor C_P voltage	161 V	144 V	188 V	146 V
Capacitor C_N voltage	159 V	143 V	185 V	144 V
THD of V_{AB}	65.9 %	47.8 %	94.6 %	51.4 %
THD of I_A	2.55 %	1.76 %	2.87 %	1.88 %

The capacitor voltages V_{CP} and V_{CN} and their currents I_{CP} and I_{CN} in two switching periods are shown in Figs. 9(f) and 10(f). In these figures, the UST state can be determined by zero current of I_{CP} and negative current of I_{CN} and vice versa for LST state. As mentioned in section III, part B, the N-type small vectors are adopted in switching sequence when V_{CN} is larger than V_{CP}. It can be recognized by only utilizing UST state instead of LST state as shown in Figs. 9(f) and 10(f). In contrast, the LST state is appeared instead of UST state when V_{CP} is larger than V_{CN}, which demonstrates that the P-type small vectors are applied in switching sequence. By this way, the capacitor voltages can be balanced in switching period as illustrated in Figs. 9(f) and 10(f).

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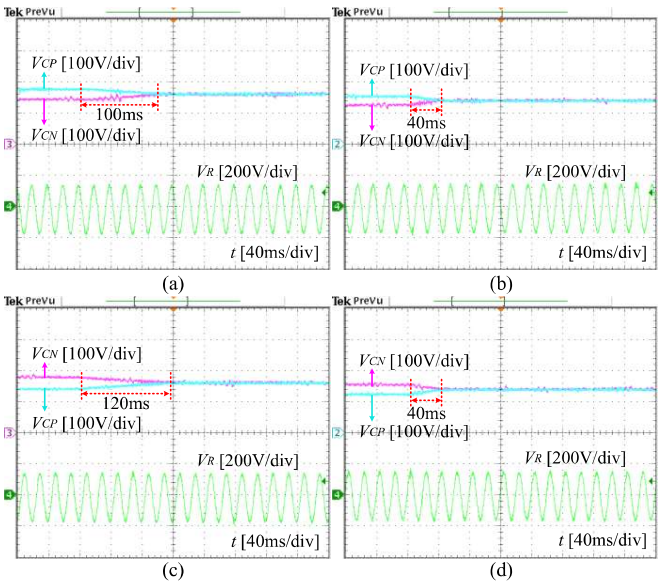

Fig. 11. Experimental results with neutral voltage balance when (a), (b) $V_{CP} > V_{CN}$, (c), (d) $V_{CP} < V_{CN}$, for (a), (c) method in [20], (b), (d) proposed method.

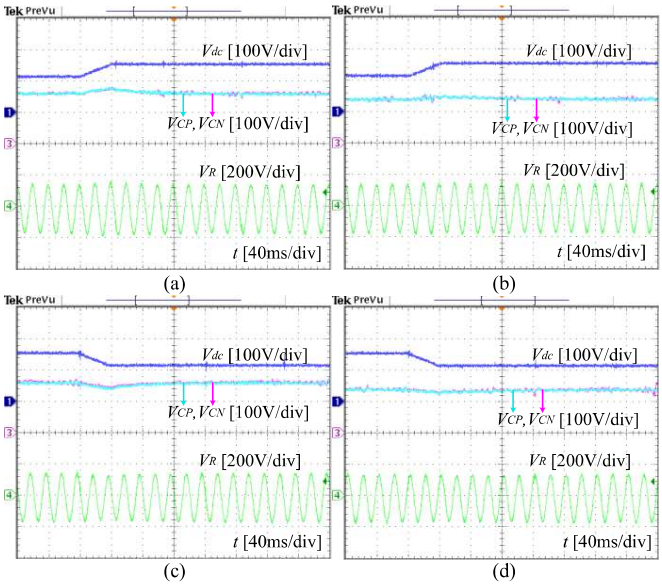

Fig. 12. Experimental results with overall control method for (a), (c) method in [20], (b), (d) proposed method.

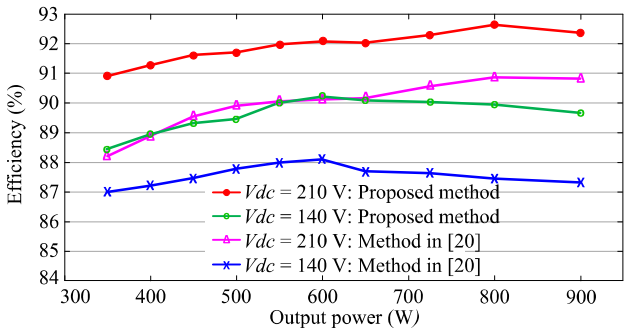

Fig. 13. Efficiency comparison between proposed method and method in [20].

The neutral-point voltage balance method is further validated in two cases: 1) when the upper capacitor voltage is larger than the lower capacitor voltage as shown in Figs. 11(a) and 11(b) and 2) the lower capacitor voltage is larger than the upper capacitor voltage as presented in Figs. 11(c) and 11(d) for both methods. In both cases, the neutral voltage is balanced with a very small difference between them. However, the proposed method has smaller time interval to recover the neutral voltage balance condition. The recovery time of the proposed method approximates 40 ms for both cases as presented in Figs. 11(b) and 11(d), whereas it is around 100 ms for case 1 and 120 ms for case 2 as shown in Fig.s 11(a) and 11(c), respectively.

The overall control methods introduced in the section III.D and in the work [20] are validated in two cases: 1) the input voltage increases from 120 V to 160 V and 2) the input source decreases from 160 V to 120 V as shown in Figs. 12(a) and 12(b) and Figs. 12(c) and 12(d), respectively. In both cases, two capacitors voltages are maintained at 165 V and 144 V for method in [20] and the proposed method, respectively. The neutral-point voltage balance is guaranteed for both methods, in two cases. With this value of capacitor voltage, the output load voltage is kept constant at 110 V_{RMS} without the variation of the input voltage. In general, the dynamic operations of both methods are the same. However, the proposed method produces a smaller overshoot than the work in [20].

The efficiency of 3L-qSBT^{2}I with the proposed SVM method and PWM method in [20] is presented in Fig. 13 when the output phase voltage is maintained at 110 V_{RMS}. These results are measured by Yokogawa WT3000E power analyzer. The proposed SVM strategy produces a higher efficiency than that of the PWM strategy in [20] as shown in Fig. 13. A maximum efficient increment of 2% is achieved with the proposed SVM method. This outstanding advantage can be explained by two main reasons as follows. Firstly, the conduction loss generated in ST state of the proposed SVM scheme is smaller than the method in [20]. This superior is achieved because the proposed method adopts smaller ST duty ratio (D_{ST}) than the method in [20]. Secondly, the switching loss of the proposed scheme is also less than the scheme in [20]. This is because the introduced SVM method needs only two communications to move from NST state to UST state or ST state, whereas it is six for the PWM method in [20]. Furthermore, the number of communications in NST state of the proposed scheme is four while it is six for the work in [20]. The efficiency of the inverter is not high because the inverter prototype is not optimal. Moreover, the use of many active switches and diodes in the circuit results in high conduction loss during ST state operation.

VI. Conclusion

This paper has presented a new SVM strategy for 3L-qSBT^{2}I which enhances output voltage gain and its quality. Under the proposed SVM scheme, the voltage stress of intermediate network components such as capacitors, switches, and diodes are significantly decreased. The P-type

and N-type small vectors are correspondingly selected to guarantee the neutral voltage balance condition. The ST states are inserted into small vectors to ensures the boost capability and ST immunity without effect of the active vectors of the inverter. However, the use of small vectors increases the common-mode voltage in the proposed method. To prove the effectiveness of the proposed SVM method, a comparison between the 3L-qSBT^{2}I with proposed SVM method and other topologies is conducted. The introduced SVM method was validated through laboratory prototype. The experimental result shows that the efficiency of the proposed SVM scheme is 2% higher than the traditional PWM technique.

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